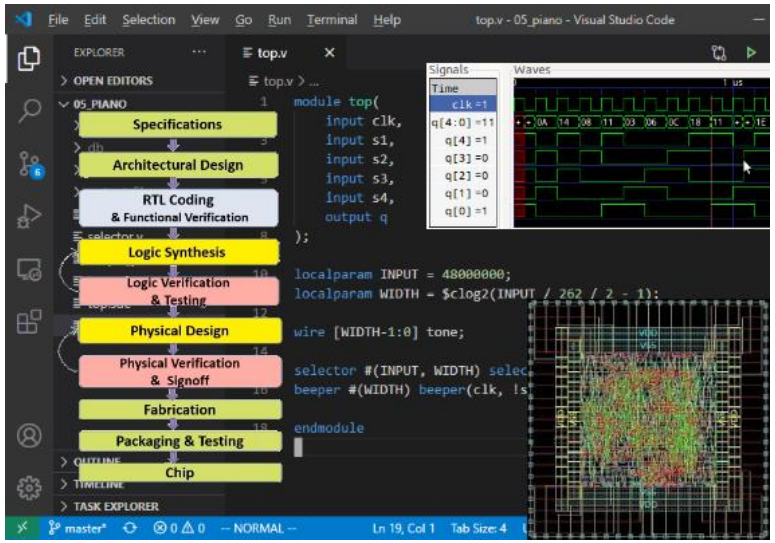
МИЭТ
Национальный исследовательский университет «МИЭТ»
Институт интегральной электроники

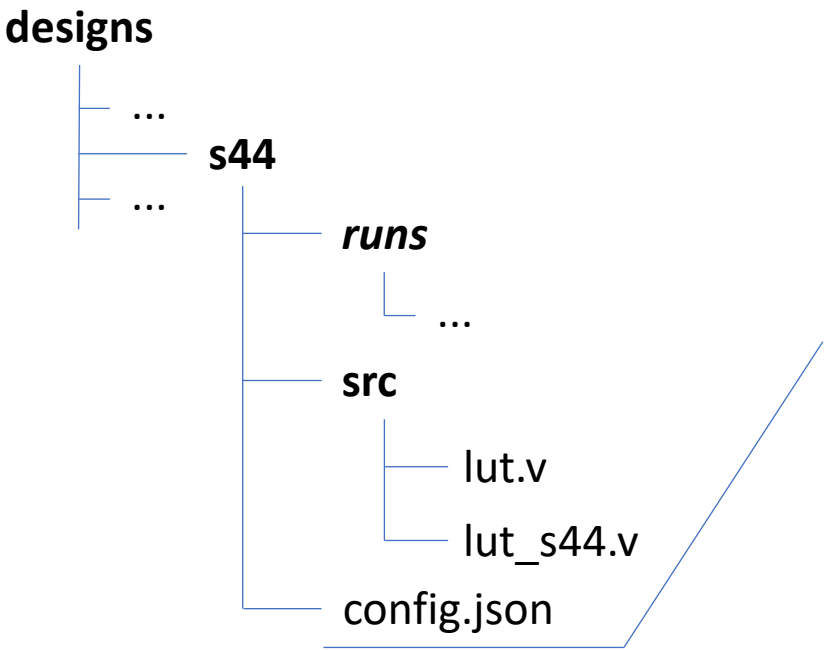
Лингвистические средства проектирования



Лекция 10

Физический синтез. Подготовка данных для фотошаблонов

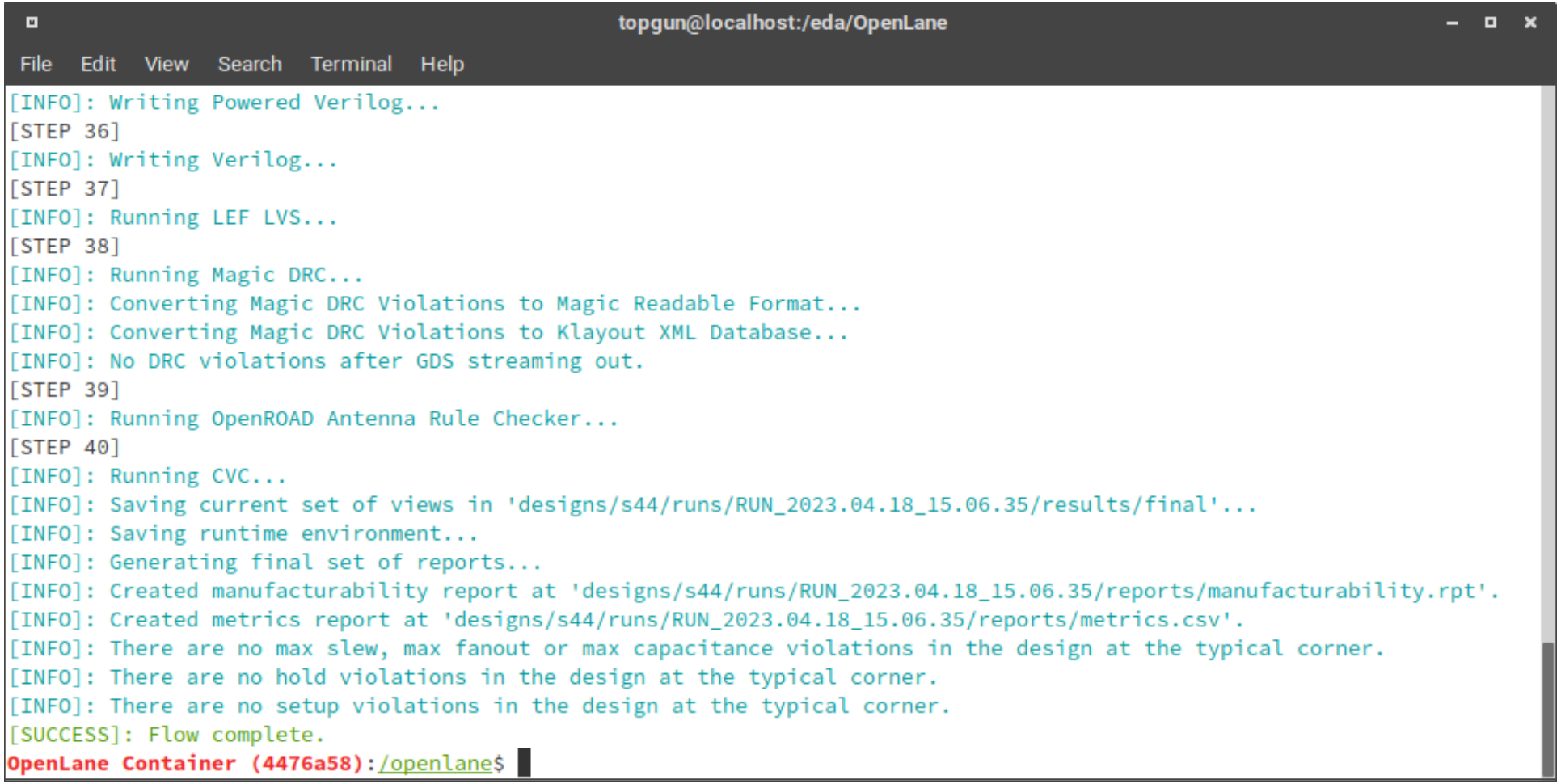
Запуск OpenLane: структура папки с проектом




```
{
    "DESIGN_NAME": "lut_s44",
    "CLOCK_PERIOD": 30,
    "VERILOG_FILES": [
        "dir::src/lut.v",
        "dir::src/lut_s44.v"
    ],
    "CLOCK_PORT": "config_clk",
    "CLOCK_NET": "config_clk",
    "FP_CORE_UTIL": 4,
    "PL_TARGET_DENSITY": 0.5,
    "DIODE_INSERTION_STRATEGY": 0,
    "USE_ARC_ANTENNA_CHECK": 1
}
```

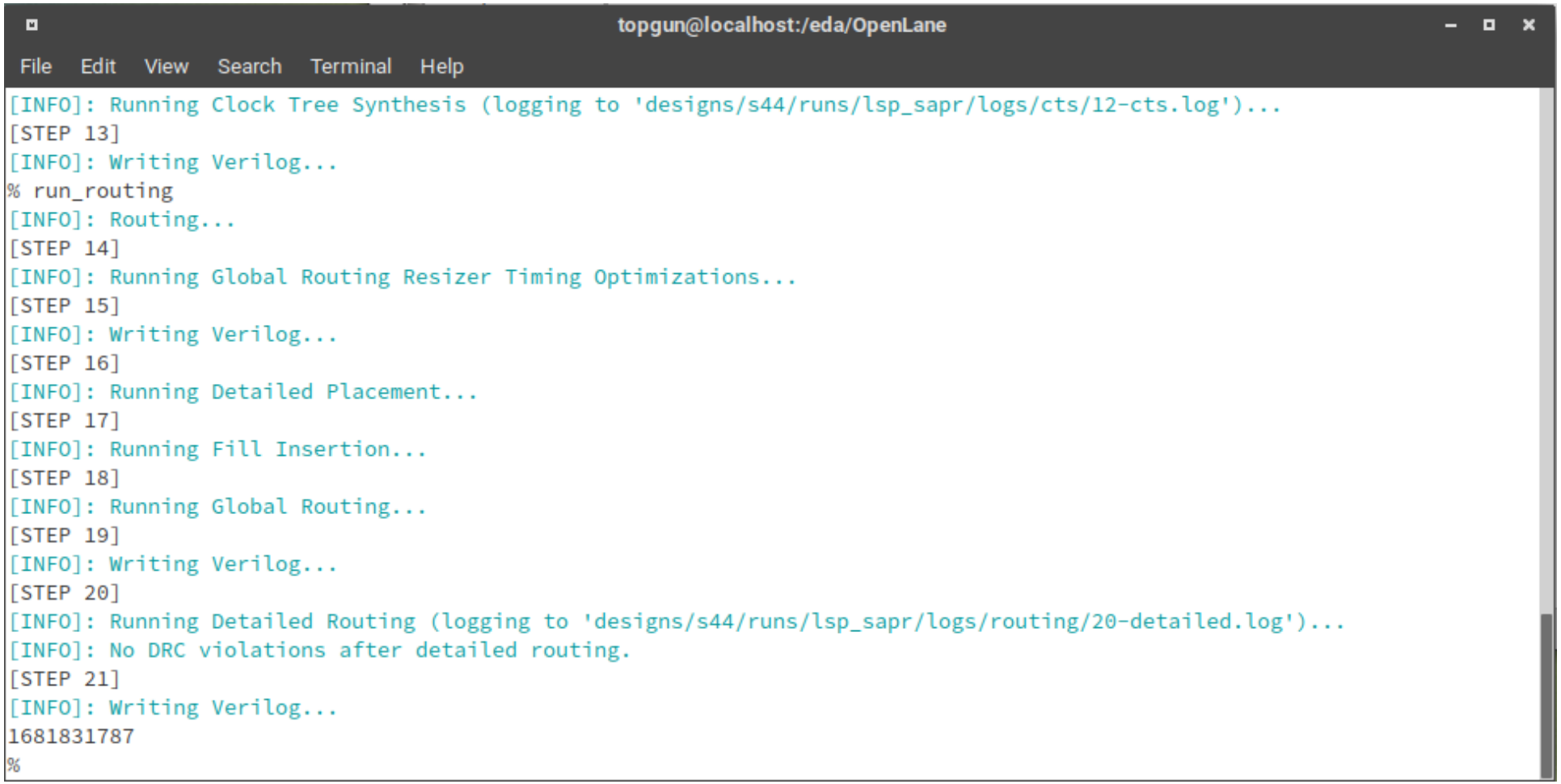
Запуск OpenLane в автоматическом режиме

```
./flow.tcl -design s44 -overwrite
```



Запуск OpenLane в интерактивном режиме

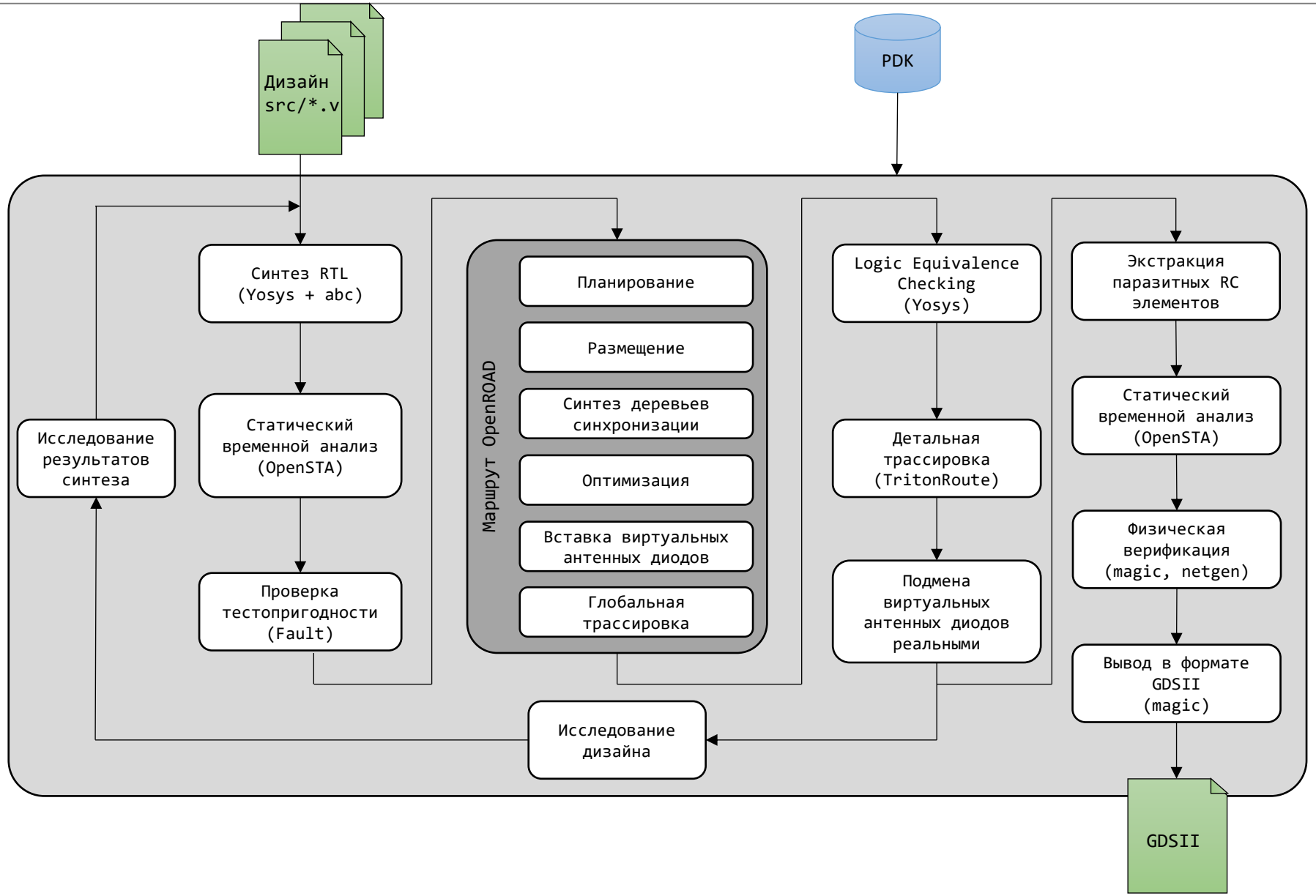
```
./flow.tcl -interactive
```



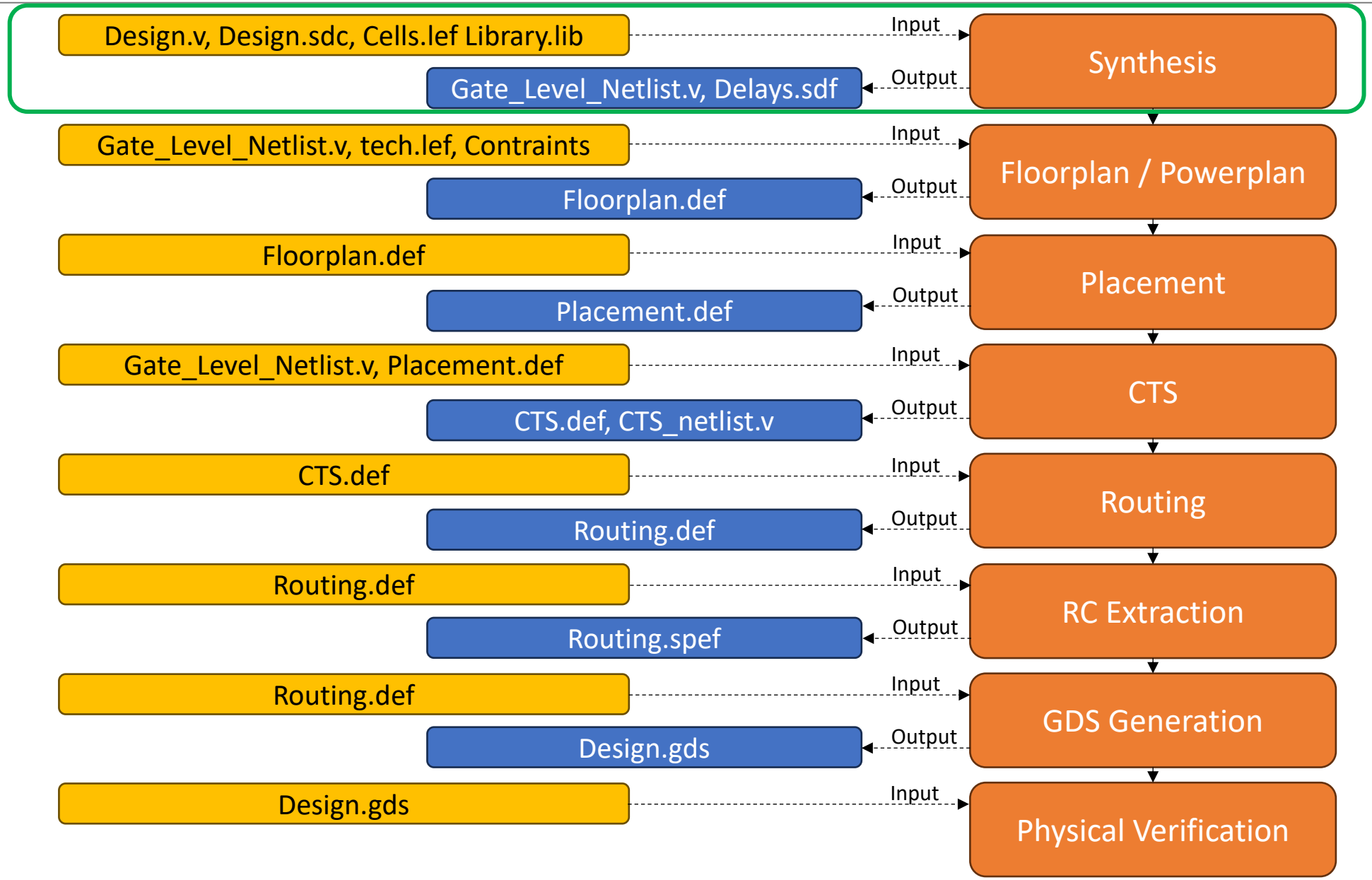
Шаги интерактивного режима

1. prep -design <design> -tag <tag>
2. run_synthesis
3. run_floorplan
4. run_placement
5. run_cts
6. run_routing
7. write_powered_verilog
8. run_magic
9. run_magic_spice_export
10. run_magic_drc
11. run_lvs
12. run_antenna_check

Последовательность выполнения проектных процедур в маршруте OpenLane



Этапы открытого маршрута OpenLane: синтез



Process Design Kit (PDK): состав

skywater-pdk / libraries /

Add file ···

QuantamHD Adding ReRAM PDK to the submodules directory of the skywater repo ✓ 68a2c36 · 3 years ago History

Name	Last commit message	Last commit date
..		
sky130_fd_io	**IO and periphery cells**	4 years ago
sky130_fd_pr	**Primitive Models and Cells**	4 years ago
sky130_fd_pr_reram	**ReRAM**	3 years ago
sky130_fd_sc_hd	**High Density Digital Standard Cells**	4 years ago
sky130_fd_sc_hdll	**High Density Low Leakage Digital Standard Cells**	4 years ago
sky130_fd_sc_hs	**High Speed Digital Standard Cells**	4 years ago
sky130_fd_sc_hvl	**High Voltage Digital Standard Cells**	4 years ago
sky130_fd_sc_lp	**Low Power Digital Standard Cells**	4 years ago
sky130_fd_sc_ls	**Low Speed Digital Standard Cells**	4 years ago
sky130_fd_sc_ms	**Medium Speed Digital Standard Cells**	4 years ago

*https://github.com/google/skywater-pdk/tree/main/libraries

Process Design Kit (PDK) : состав библиотеки

skywater-pdk-libs-sky130_fd_sc_hd Public

ac7fb61 | 4 Branches | 3 Tags | Go to file t | Code

mithro lpflow_bleeder: Fixing the verilog models. ac7fb61 · 4 years ago | 55 Commits

cells	lpflow_bleeder: Fixing the verilog models.	4 years ago
models	verilog: Fixing ordering of ports in primitives.	4 years ago
tech	Fixing the technology LEF file.	4 years ago
timing	Convert to using comma seperator in .lib.json files.	4 years ago
.gitignore	Adding .gitignore file.	4 years ago
LICENSE	Initial empty repository.	4 years ago
README.rst	Significant improvements to library sky130_fd_sc_hd version ...	4 years ago

Process Design Kit (PDK): UDP (1)

skywater-pdk-libs-sky130_fd_sc_hd / models /

kevink78 Significant improvements to library

Name	
..	
definition.json	
sky130_fd_sc_hd__udp_mux_2to1.blackbox.v	
sky130_fd_sc_hd__udp_mux_2to1.symbol.svg	
sky130_fd_sc_hd__udp_mux_2to1.symbol.v	Significant im
sky130_fd_sc_hd__udp_mux_2to1.table.tsv	Significant im
sky130_fd_sc_hd__udp_mux_2to1.tb.v	Significant im
sky130_fd_sc_hd__udp_mux_2to1.v	Significant im

```
(* blackbox *)
module sky130_fd_sc_h
    X ,
    A0,
    A1,
    S
);

    output X ;
    input  A0;
    input  A1;
    input  S ;
endmodule
```

```
primitive sky130_fd_sc_hd__udp_mux_2to1 (
    X ,
    A0,
    A1,
    S
);

    output X ;
    input  A0;
    input  A1;
    input  S ;

    table
     //  A0  A1  S  :  X
         0   0   ?  :  0  ;
         1   1   ?  :  1  ;
         0   ?   0  :  0  ;
         1   ?   0  :  1  ;
         ?   0   1  :  0  ;
         ?   1   1  :  1  ;
    endtable
endprimitive
```

Process Design Kit (PDK): UDP (2)

skywater-pdk-libs-sky130_fd_sc_hd / models / udp_mux_2to1 /

```
module top();

    // Inputs are registered
    reg A0;
    reg A1;
    reg S;

    // Outputs are wires
    wire X;

    initial
    begin

    end

    sky130_fd_sc_hd__udp_mux_2to1 dut (.A0(A0),

endmodule
```

```
// Initial state is x for all inputs.
       A0 = 1'bX;
       A1 = 1'bX;
       S  = 1'bX;

       #20   A0 = 1'b0;
       #40   A1 = 1'b0;
       #60   S  = 1'b0;
       #80   A0 = 1'b1;
       #100  A1 = 1'b1;
       #120  S  = 1'b1;
       #140  A0 = 1'b0;
       #160  A1 = 1'b0;
       #180  S  = 1'b0;
       #200  S  = 1'b1;
       #220  A1 = 1'b1;
       #240  A0 = 1'b1;
       #260  S  = 1'bx;
       #280  A1 = 1'bx;
       #300  A0 = 1'bx;
```

Process Design Kit (PDK): UDP (3)

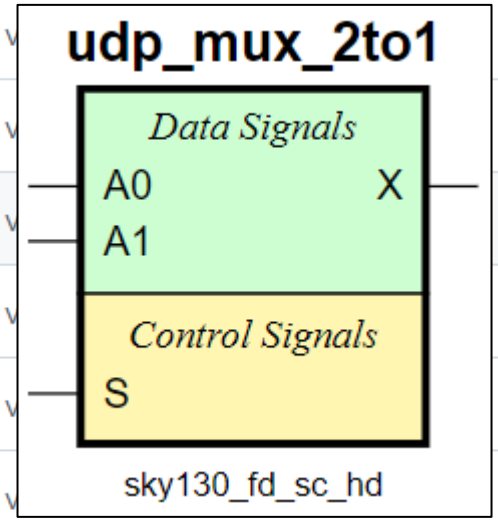
skywater-pdk-libs-sky130

Preview | Code | Blame | 7 lines (7 loc) · 94 Bytes | Raw

```
1   A0   A1   S   :   X   Comments
2   0    0    ?   :   0
3   1    1    ?   :   1
4   0    ?    0   :   0
5   1    ?    0   :   1
6   ?    0    1   :   0
7   ?    1    1   :   1
```

kevink78 Significant — ca9a95a · 4 years ago — History

Name	Last commit date
..	
definition.json	4 years ago
sky130_fd_sc_hd__udp_mux_2to1.blackbox.v	Significant improvements to library sky130_fd_sc_hd v… 4 years ago
sky130_fd_sc_hd__udp_mux_2to1.symbol.svg	Significant improvements to library sky130_fd_sc_hd v… 4 years ago
sky130_fd_sc_hd__udp_mux_2to1.symbol.v	Significant improvements to library sky130_fd_sc_hd v… 4 years ago
sky130_fd_sc_hd__udp_mux_2to1.table.tsv	Significant improvements to library sky130_fd_sc_hd v… 4 years ago
sky130_fd_sc_hd__udp_mux_2to1.tb.v	Significant improvements to library sky130_fd_sc_hd v… 4 years ago
sky130_fd_sc_hd__udp_mux_2to1.v	Significant improvements to library sky130_fd_sc_hd v… 4 years ago



Process Design Kit (PDK): ячейки (1)

skywater-pdk-libs-sky130_fd_sc_hd / cells /

mithro lpflow_bleeder: Fixing the verilog models. ac7fb61 · 4 years ago History

Name	Last commit message	Last commit date
..		
a2111o	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a2111oi	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a211o	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a211oi	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a21bo	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a21boi	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a21o	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a21oi	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago
a221o	lef: Fixing VNB/VPB properties in .magic.lef files.	4 years ago

Process Design Kit (PDK): ячейки (2)

skywater-pdk-libs-sky130_fd_sc_hd / cells / a22o /

mithro lef: Fixing VNB/VPB properties in .magic.lef files.

Name	Last commit message	
..		
definition.json	Significant improvement	
sky130_fd_sc_hd__a22o.behavioral.pp.v	Significant improvement	
sky130_fd_sc_hd__a22o.behavioral.v	Significant improvement	
sky130_fd_sc_hd__a22o.blackbox.v	Significant improvement	
sky130_fd_sc_hd__a22o.functional.pp.v	Significant improvement	
sky130_fd_sc_hd__a22o.functional.v	Significant improvement	
sky130_fd_sc_hd__a22o.json	Significant improvement	
sky130_fd_sc_hd__a22o.pp.blackbox.v	Significant improvement	
sky130_fd_sc_hd__a22o.pp.symbol.svg	Significant improvement	
sky130_fd_sc_hd__a22o.pp.symbol.v	Significant improvement	
sky130_fd_sc_hd__a22o.schematic.svg	Significant improvements to library sky130_fd_sc_hd version 0.0.1.	4 years ago

```
module sky130_fd_sc_hd__a22o (X, A1, A2, B1, B2);
    output X ;
    input  A1;
    input  A2;
    input  B1;
    input  B2;

    supply1 VPWR;
    supply0 VGND;
    supply1 VPB ;
    supply0 VNB ;

    wire and0_out ;
    wire and1_out ;
    wire or0_out_X;

    and and0 (and0_out , B1, B2            );
    and and1 (and1_out , A1, A2            );
    or  or0  (or0_out_X, and1_out, and0_out);
    buf buf0 (X        , or0_out_X         );

endmodule
```

Process Design Kit (PDK): ячейки (4)

skywater-pdk-libs-sky130_fd_sc_hd / cells / a22o /

mithro lef: Fixing VNB/VPB properties in .magic.lef files.

Name
..
definition.json
sky130_fd_sc_hd__a22o.behavioral.pp.v
sky130_fd_sc_hd__a22o.behavioral.v
sky130_fd_sc_hd__a22o.blackbox.v
sky130_fd_sc_hd__a22o.functional.pp.v
sky130_fd_sc_hd__a22o.functional.v
sky130_fd_sc_hd__a22o.json
sky130_fd_sc_hd__a22o.pp.blackbox.v
sky130_fd_sc_hd__a22o.pp.symbol.svg
sky130_fd_sc_hd__a22o.pp.symbol.v
sky130_fd_sc_hd__a22o.schematic.svg

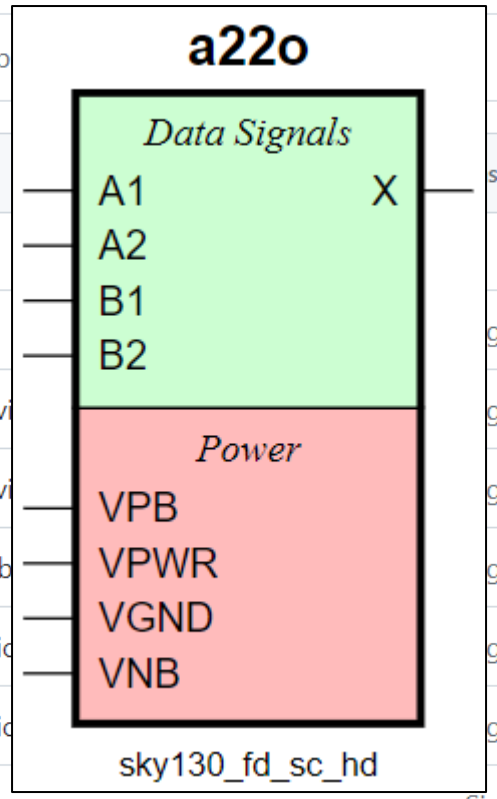
```
.SUBCKT sky130_fd_sc_hd__a22o_1 A1 A2 B1 B2 VGND VNB VPB VPWR X
*.PININFO A1:I A2:I B1:I B2:I VGND:I VNB:I VPB:I VPWR:I X:O
MMPA0 pndA A1 VPWR VPB pfet_01v8_hvt m=1 w=1.0 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMPA1 pndA A2 VPWR VPB pfet_01v8_hvt m=1 w=1.0 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMPB0 y B1 pndA VPB pfet_01v8_hvt m=1 w=1.0 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMPB1 y B2 pndA VPB pfet_01v8_hvt m=1 w=1.0 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMIPX X y VPWR VPB pfet_01v8_hvt m=1 w=1.0 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMNA0 y A1 sndA1 VNB nfet_01v8 m=1 w=0.65 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMNA1 sndA1 A2 VGND VNB nfet_01v8 m=1 w=0.65 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMNB0 y B1 sndB1 VNB nfet_01v8 m=1 w=0.65 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMNB1 sndB1 B2 VGND VNB nfet_01v8 m=1 w=0.65 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
MMINX X y VGND VNB nfet_01v8 m=1 w=0.65 l=0.15 mult=1 sa=0.265
+ sb=0.265 sd=0.28 topography=normal area=0.063 perim=1.14
.ENDS sky130_fd_sc_hd__a22o_1
```

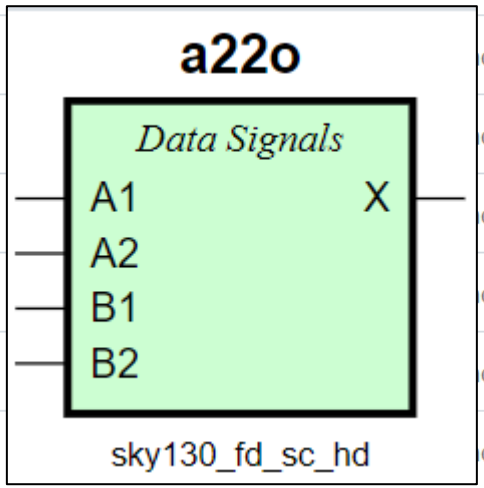
Process Design Kit (PDK): ячейки (5)

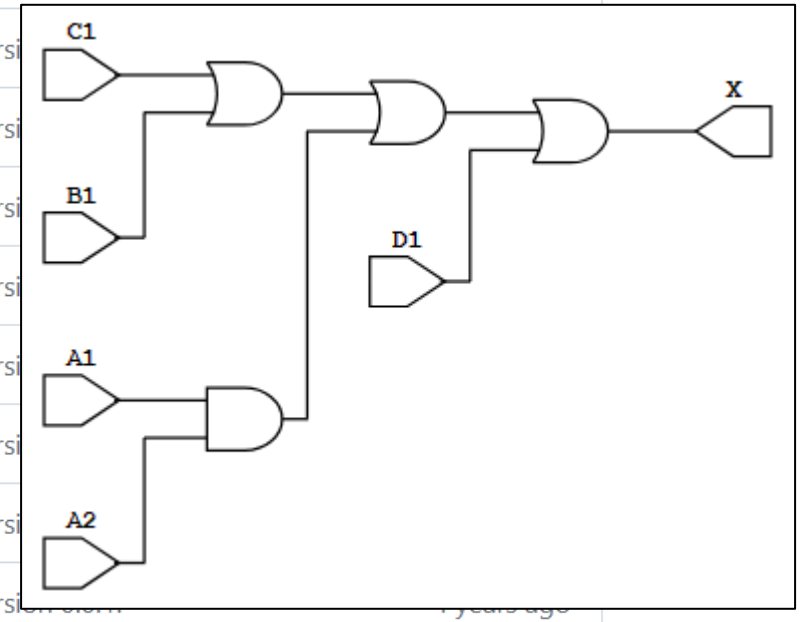
skywater-pdk-libs-sky130_fd_sc_hd / cells / a22o /

mithro lef: Fixing VNB/VPB p 3aaa84e · 4 years ago History

Name	st commit message	Last commit date
..		
definition.json	gnificant d version 0.0.1.	4 years ago
sky130_fd_sc_hd__a22o.behavi	gnificant d version 0.0.1.	4 years ago
sky130_fd_sc_hd__a22o.behavi	gnificant d versi	
sky130_fd_sc_hd__a22o.blackb	gnificant d versi	
sky130_fd_sc_hd__a22o.functic	gnificant d versi	
sky130_fd_sc_hd__a22o.functic	gnificant d versi	
sky130_fd_sc_hd__a22o.json	Significant improvements to library sky130_fd_sc_hd versi	
sky130_fd_sc_hd__a22o.pp.blackbox.v	Significant improvements to library sky130_fd_sc_hd versi	
sky130_fd_sc_hd__a22o.pp.symbol.svg	Significant improvements to library sky130_fd_sc_hd versi	
sky130_fd_sc_hd__a22o.pp.symbol.v	Significant improvements to library sky130_fd_sc_hd versi	
sky130_fd_sc_hd__a22o.schematic.svg	Significant improvements to library sky130_fd_sc_hd version 0.0.1.	4 years ago

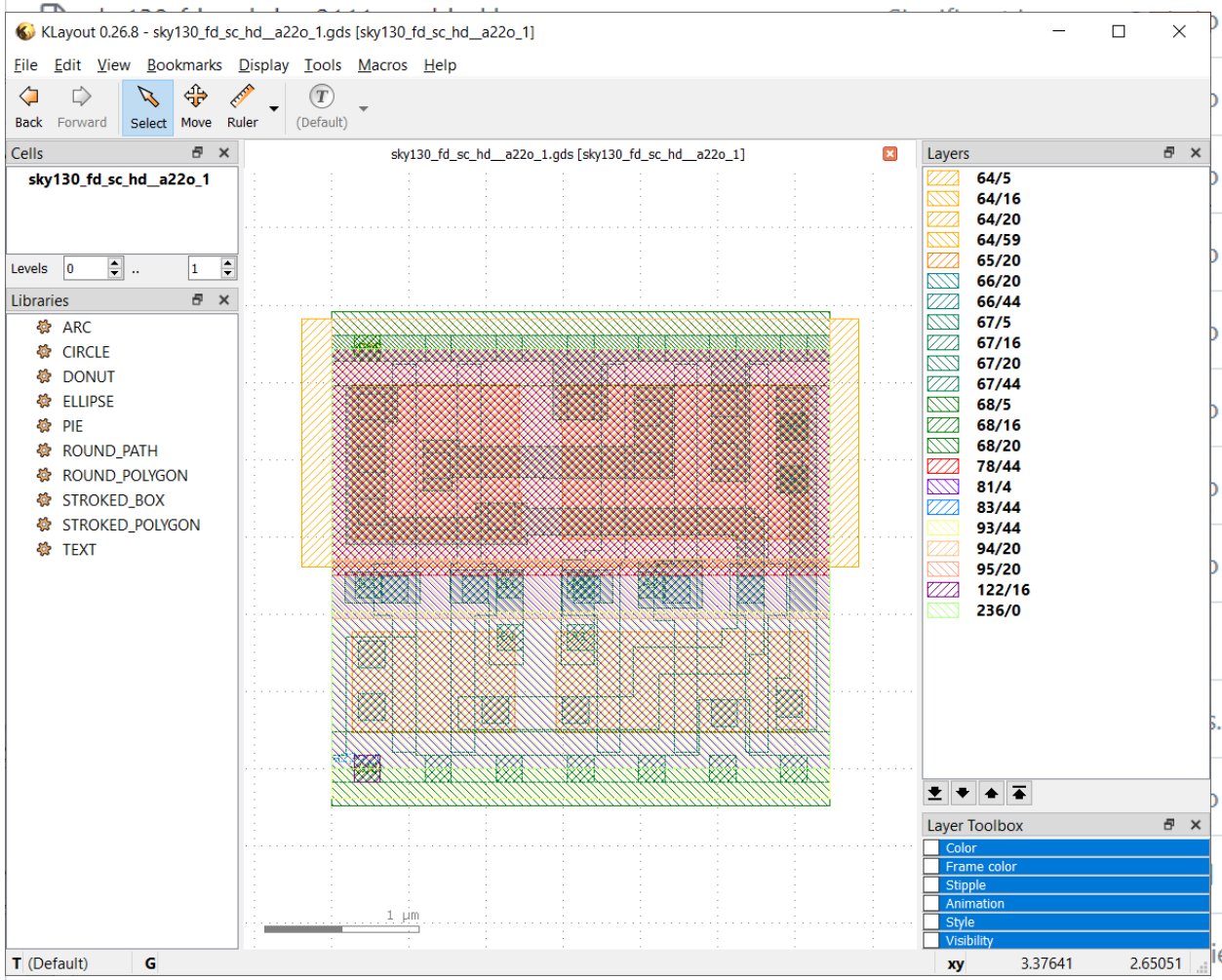


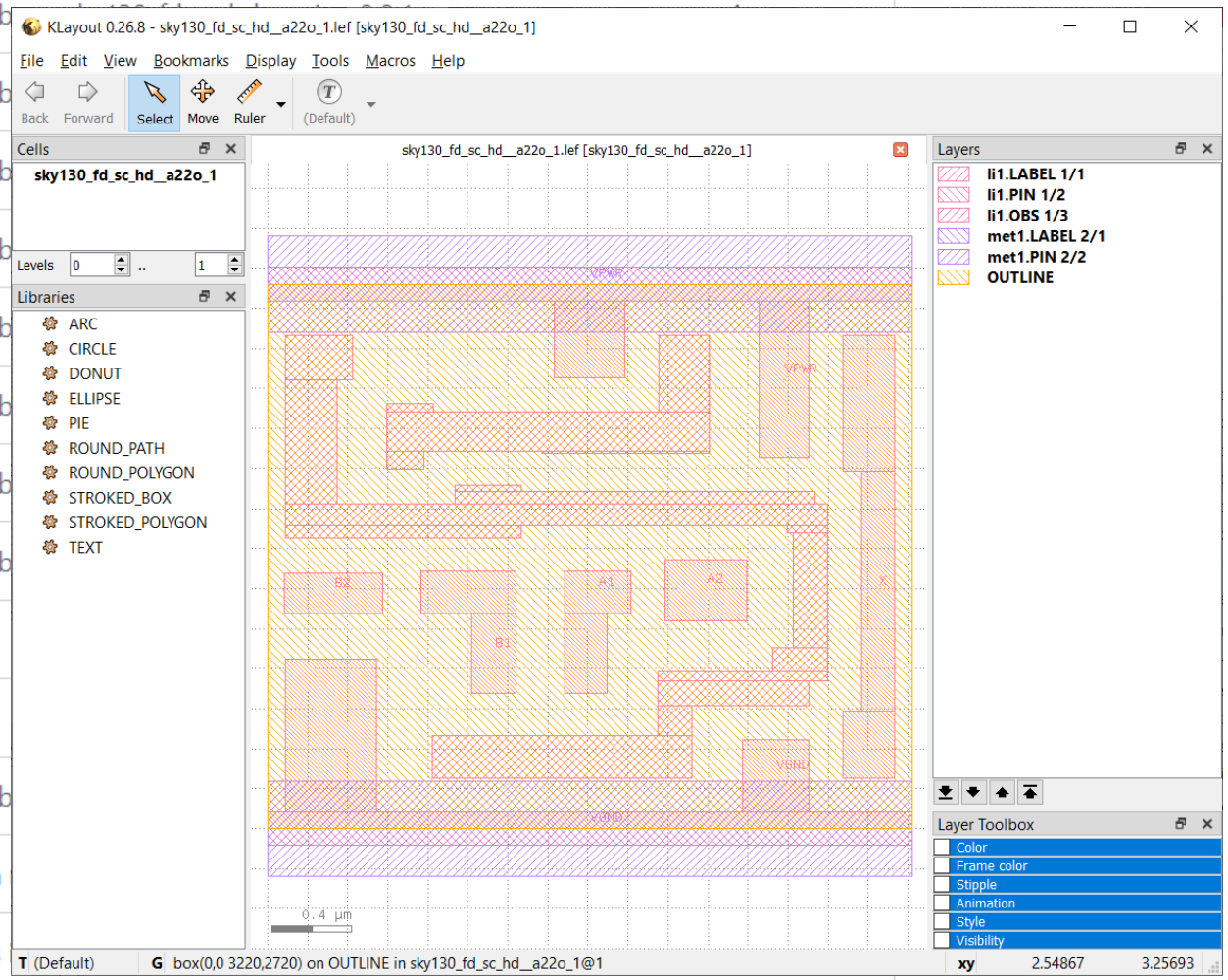




Process Design Kit (PDK): топологии ячеек

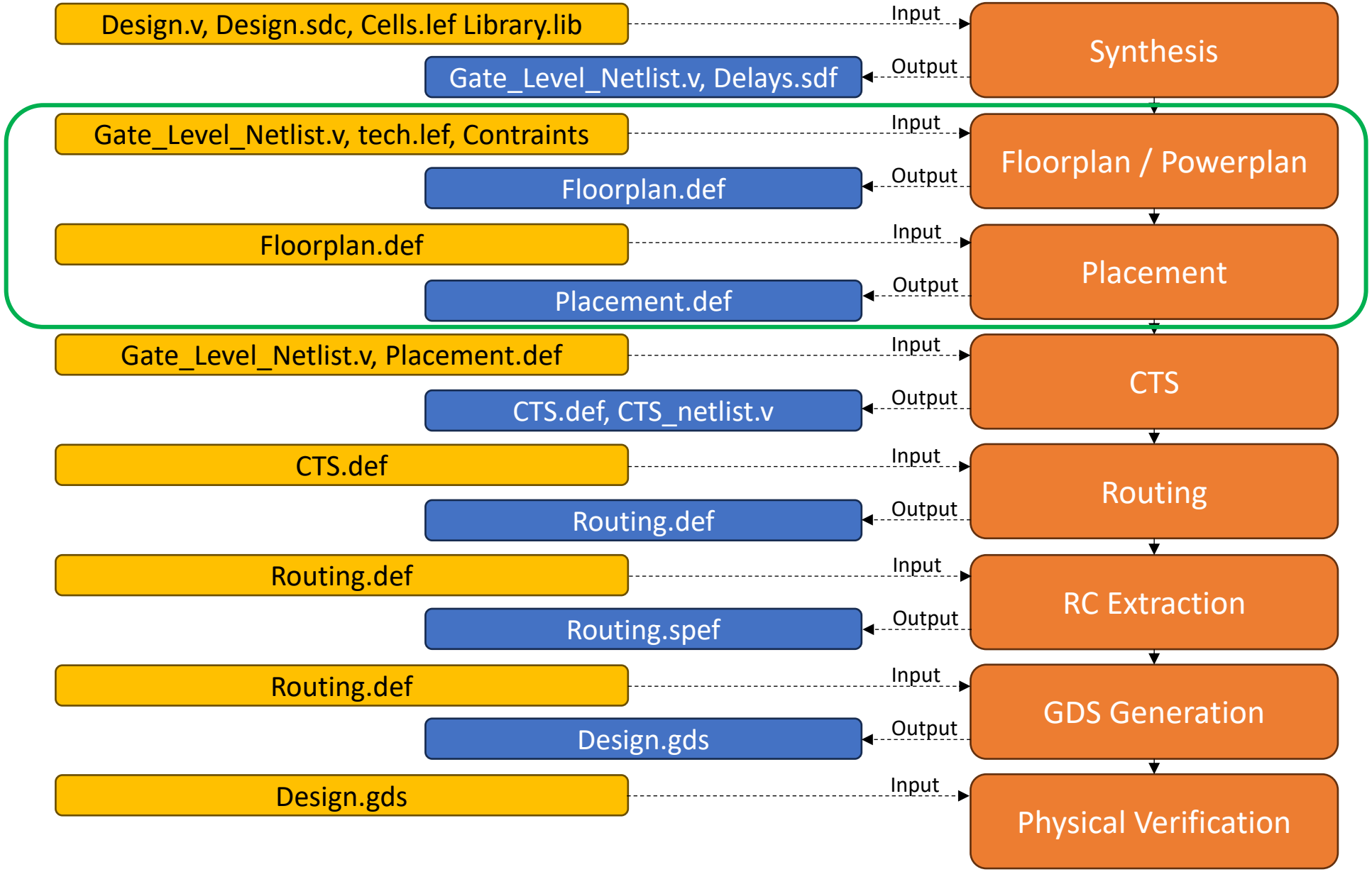
skywater-pdk-libs-sky130_fd_sc_hd / cells / a2111o / ↑ Top



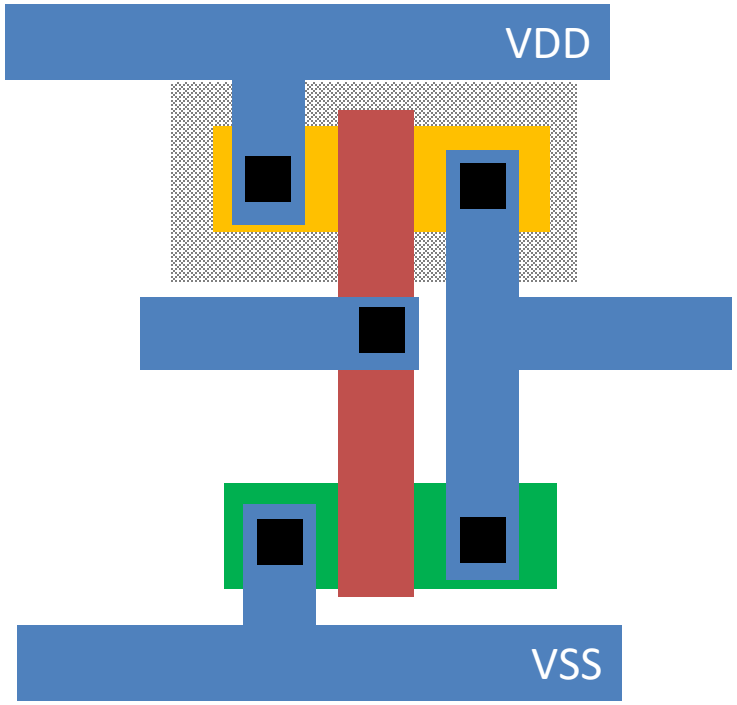


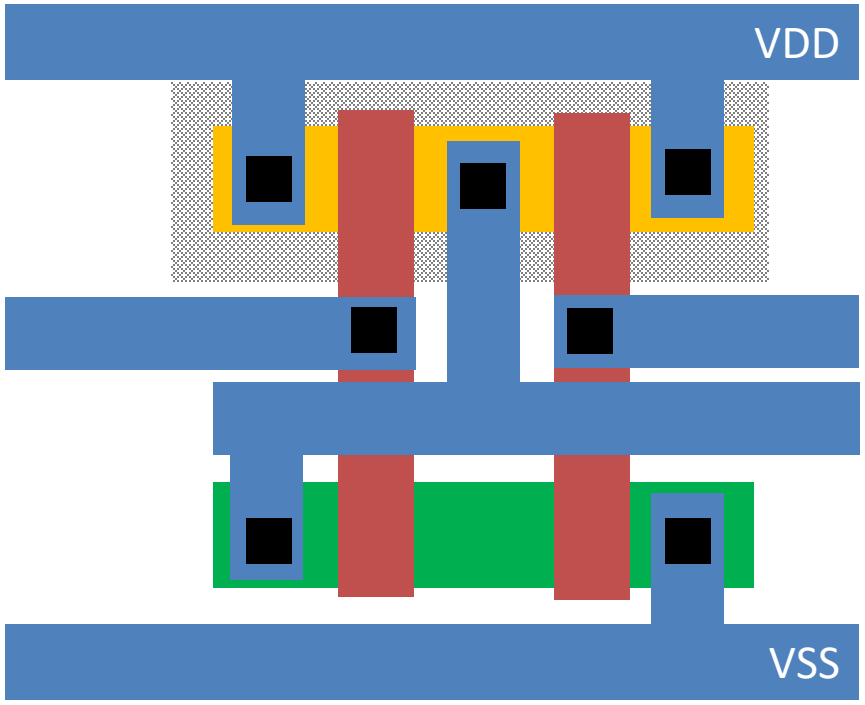
sky130_fd_sc_hd__a2111o_1.netlist.tsv Updating spice files for names in pending `sky130_fd_pr` release. 4 years ago

Этапы открытого маршрута OpenLane: планирование и размещение

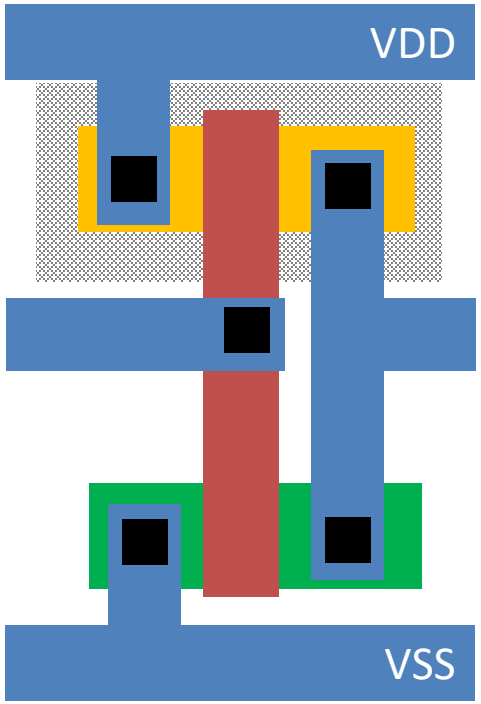


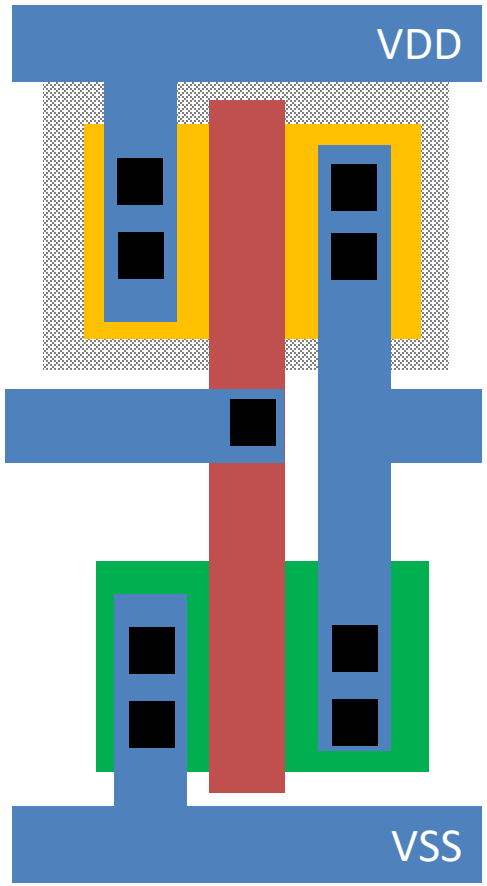
Стандартные ячейки для различных логических функций

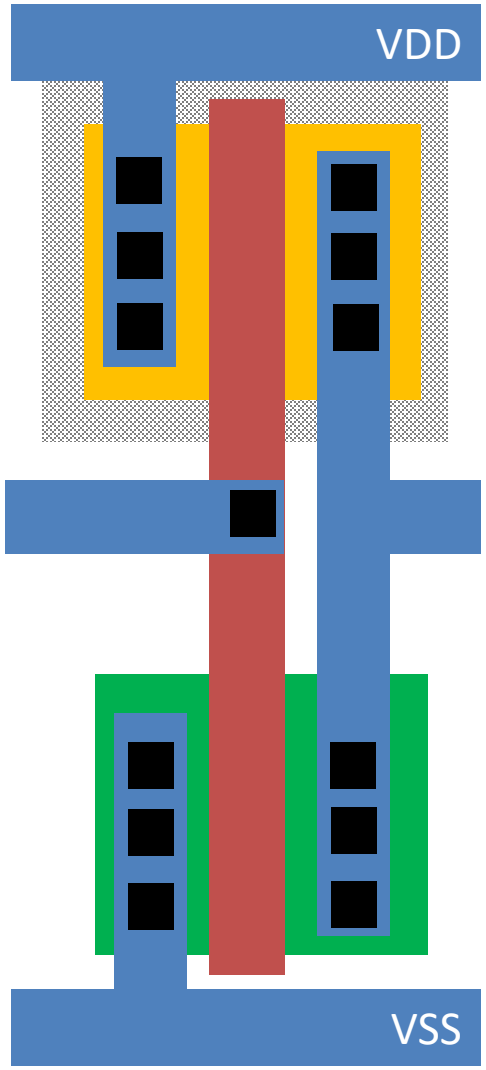




Варьирование высоты стандартных ячеек







Описание стандартных ячеек: формат LEF (1)

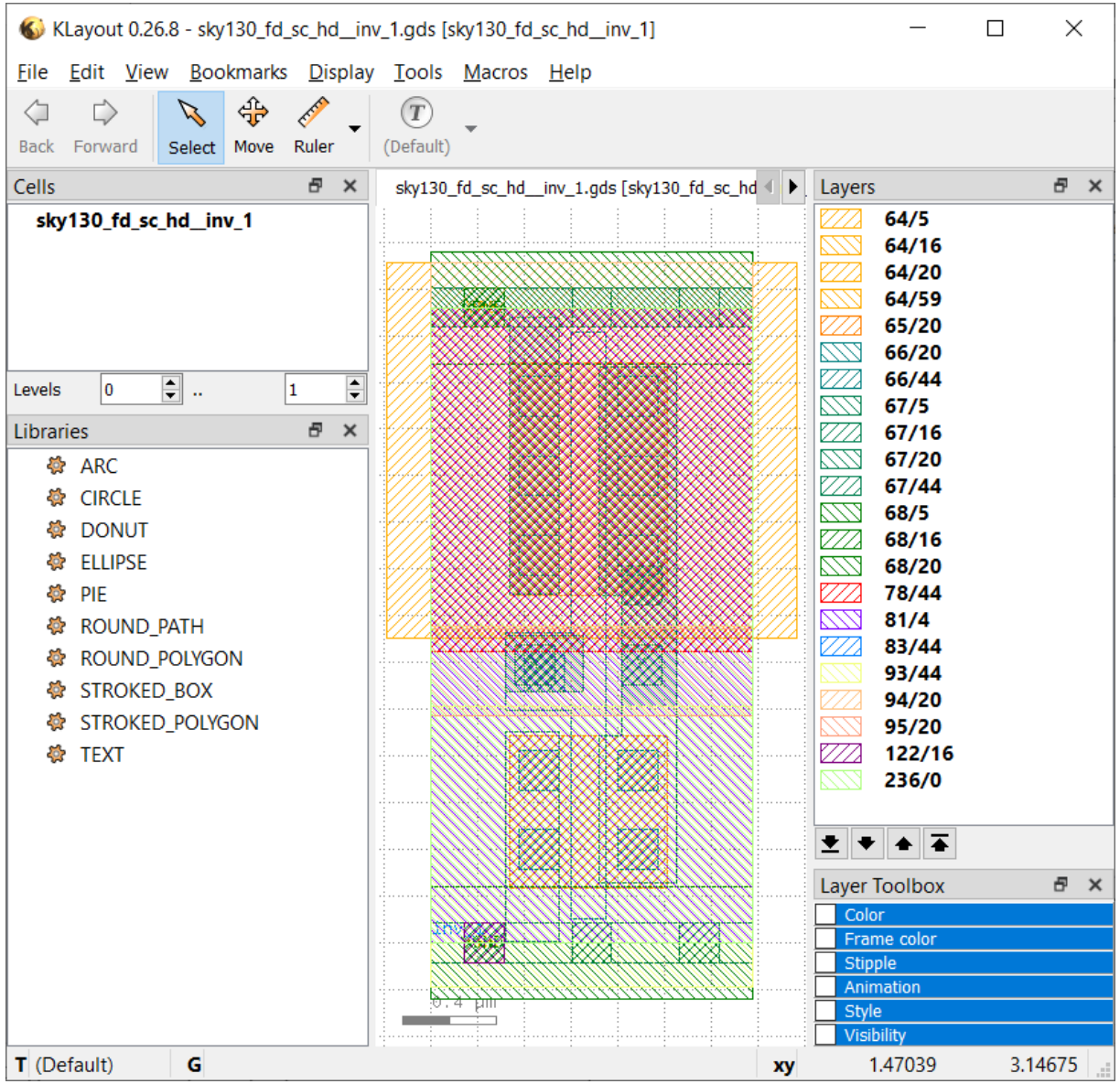
skywater

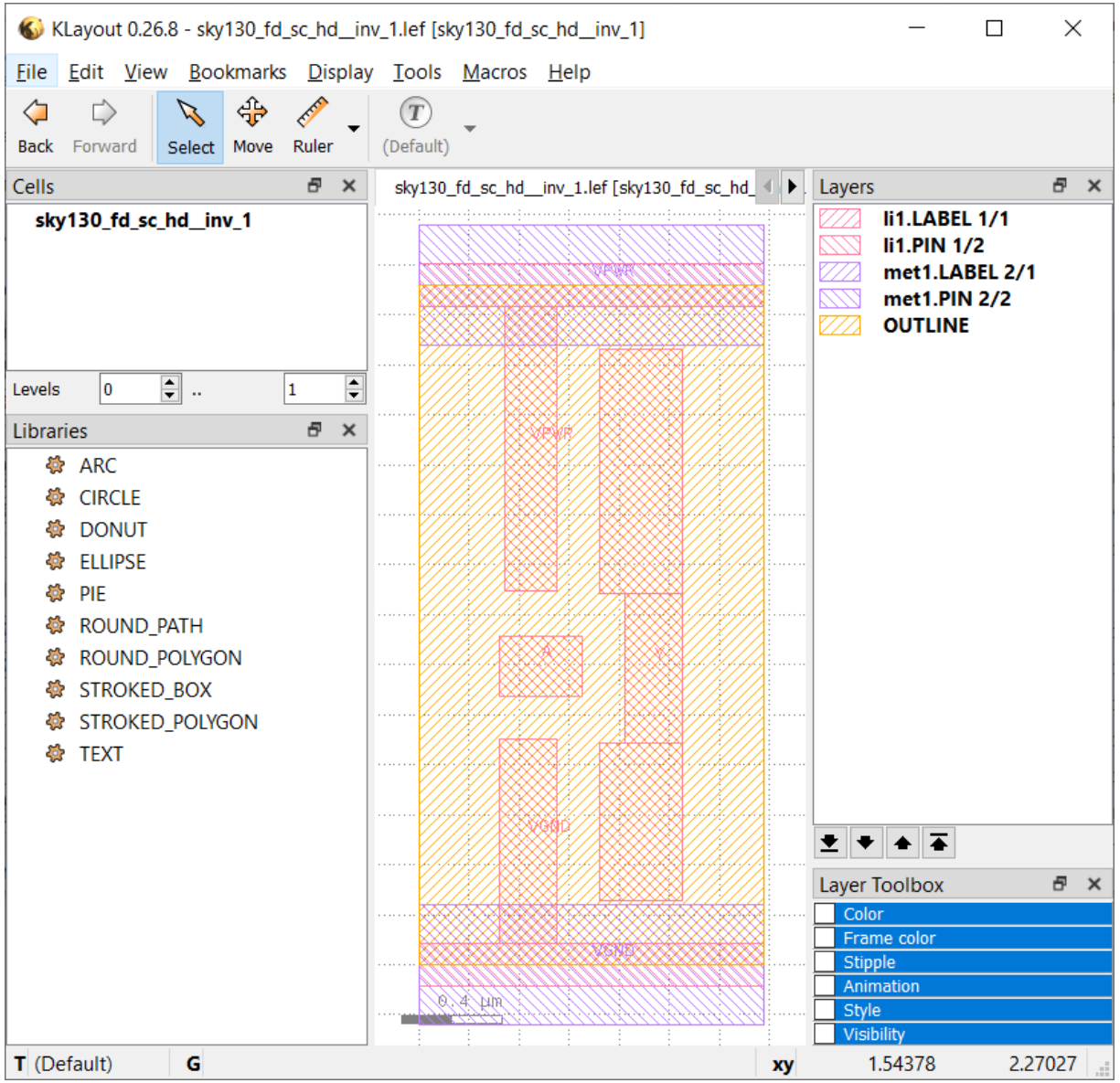
```
VERSION 5.5 ;
NAMESCASESENSITIVE ON ;
BUSBITCHARS "[]" ;
DIVIDERCHAR "/" ;

MACRO sky130_fd_sc_hd__inv_1
  CLASS CORE ;
  SOURCE USER ;
  ORIGIN  0.000000  0.000000 ;
  SIZE  1.380000 BY  2.720000 ;
  SYMMETRY X Y R90 ;
  SITE unithd ;

  ...

END sky130_fd_sc_hd__inv_1
```

Описание стандартных ячеек: формат LEF (2)

```
VERSION 5.5 ;
NAMESCASESENSITIVE ON ;
BUSBITCHARS "[]" ;
DIVIDERCHAR "/" ;

MACRO sky130_fd_sc_hd__inv_1
  CLASS CORE ;
  ...

  PIN A
    ANTENNAGATEAREA  0.247500 ;
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER li1 ;
        RECT 0.320000 1.075000 0.650000 1.315000 ;
    END
  END A


END sky130_fd_sc_hd__inv_1
```

GDSII vs LEF


KLayout 0.26.8 - sky130_fd_sc_hd__inv_1.gds [sky130_fd_sc_hd__inv_1]
File Edit View Bookmarks Display Tools Macros Help
Back Forward Select Move Ruler (Default)
Cells
sky130_fd_sc_hd__inv_1
Levels 0 .. 1
Libraries
ARC
CIRCLE
DONUT
ELLIPSE
PIE
ROUND_PATH
ROUND_POLYGON
STROKED_BOX
STROKED_POLYGON
TEXT
sky130_fd_sc_hd__inv_1.gds [sky130_fd_sc_hd
Layers
64/5
64/16
64/20
64/59
65/20
66/20
66/44
67/5
67/16
67/20
67/44
68/5
68/16
68/20
78/44
81/4
83/44
93/44
94/20
95/20
122/16
236/0
Layer Toolbox
Color
Frame color
Stipple
Animation
Style
Visibility
T (Default) G xy 1.47039 3.14675


KLayout 0.26.8 - sky130_fd_sc_hd__inv_1.lef [sky130_fd_sc_hd__inv_1]
File Edit View Bookmarks Display Tools Macros Help
Back Forward Select Move Ruler (Default)
Cells
sky130_fd_sc_hd__inv_1
Levels 0 .. 1
Libraries
ARC
CIRCLE
DONUT
ELLIPSE
PIE
ROUND_PATH
ROUND_POLYGON
STROKED_BOX
STROKED_POLYGON
TEXT
sky130_fd_sc_hd__inv_1.lef [sky130_fd_sc_hd_
VPWR
VGND
VNB
A
Y
Layers
li1.LABEL 1/1
li1.PIN 1/2
met1.LABEL 2/1
met1.PIN 2/2
OUTLINE
Layer Toolbox
Color
Frame color
Stipple
Animation
Style
Visibility
T (Default) G xy 1.54378 2.27027

Технологические данные в формате LEF (1)

```
VERSION 5.7 ;

BUSBITCHARS "[]" ;
DIVIDERCHAR "/" ;

UNITS
  TIME NANOSECONDS 1 ;
  CAPACITANCE PICOFARADS 1 ;
  RESISTANCE OHMS 1 ;
  DATABASE MICRONS 1000 ;
END UNITS

MANUFACTURINGGRID 0.005 ;

SITE unithd
  SYMMETRY Y ;
  CLASS CORE ;
  SIZE 0.46 BY 2.72 ;
END unithd
```

```
LAYER nwell
  TYPE MASTERSLICE ;
  PROPERTY LEF58_TYPE "TYPE NWELL ;" ;
END nwell

LAYER pwell
  TYPE MASTERSLICE ;
  PROPERTY LEF58_TYPE "TYPE PWELL ;" ;
END pwell
```

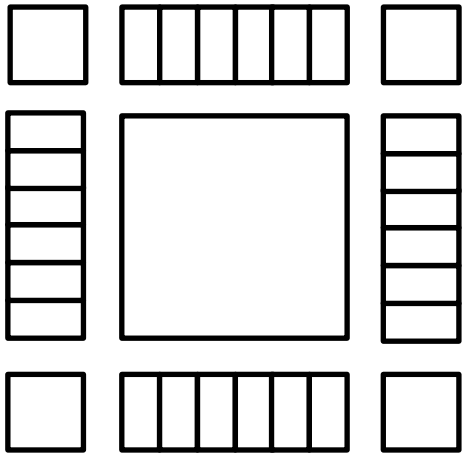
Технологические данные в формате LEF (2)

```
LAYER met1
  TYPE ROUTING ;
  DIRECTION HORIZONTAL ;

  PITCH 0.34 ;
  OFFSET 0.17 ;

  WIDTH 0.14 ;
  SPACINGTABLE
     PARALLELRUNLENGTH 0
     WIDTH 0 0.14
     WIDTH 3 0.28 ;
  AREA 0.083 ;
  THICKNESS 0.35 ;

  EDGECAPACITANCE 40.567E-6 ;
   CAPACITANCE CPERSQDIST 25.7784E-6 ;
   DCCURRENTDENSITY AVERAGE 2.8 ;
   ACCURRENTDENSITY RMS 6.1 ;
   MAXIMUMDENSITY 70 ;
   DENSITYCHECKWINDOW 700 700 ;
   DENSITYCHECKSTEP 70 ;

   RESISTANCE RPERSQ 0.125 ;
 END met1

  ANTENNAMODEL OXIDE1 ;
  ANTENNADIFFSIDEAREARATIO PWL ( ( 0 400 ) ( 0.0125 400 ) ( 0.0225 2609 ) ( 22.5 11600 ) ) ;
```

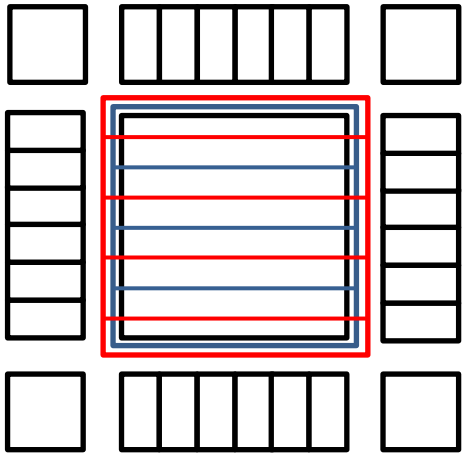
Технологические данные в формате LEF (3)

```
LAYER via
  TYPE CUT ;
  WIDTH 0.15 ;
  SPACING 0.17 ;
  ENCLOSURE BELOW 0.055 0.085 ;
  ENCLOSURE ABOVE 0.055 0.085 ;

  ANTENNADIFFAREARATIO PWL ( ( 0 6 ) ( 0.0125 6 ) ( 0.0225 6.81 ) ( 22.5 816 ) ) ;
  DCCURRENTDENSITY AVERAGE 0.29 ; # mA per via Iavg_max at Tj = 90oC
END via


LAYER via2
  TYPE CUT ;
  WIDTH 0.2 ;                  # Via2 1
  SPACING 0.2 ;                # Via2 2
  ENCLOSURE BELOW 0.04 0.085 ;  # Via2 4
  ENCLOSURE ABOVE 0.065 0.065 ; # Met3 4
  ANTENNADIFFAREARATIO PWL ( ( 0 6 ) ( 0.0125 6 ) ( 0.0225 6.81 ) ( 22.5 816 ) ) ;
  DCCURRENTDENSITY AVERAGE 0.48 ; # mA per via Iavg_max at Tj = 90oC
END via2
```

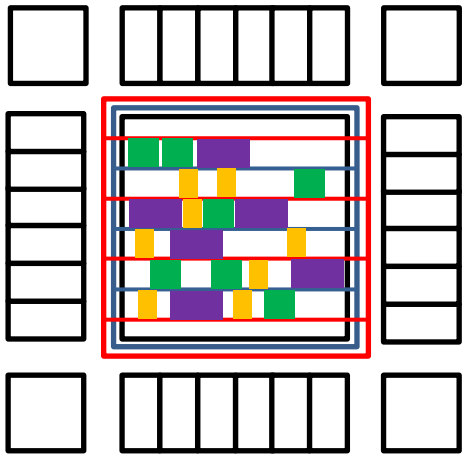
Place & Route (P&R)



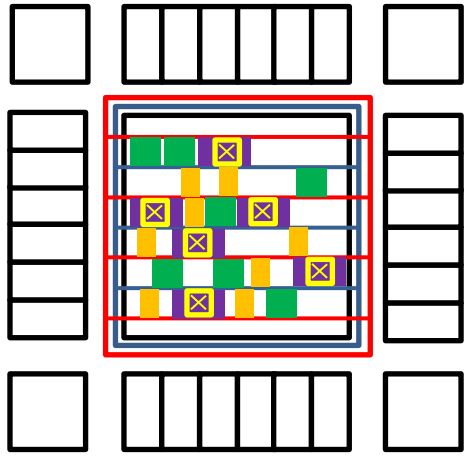
Начальное планирование кристалла
(Initial floorplan and pad ring)



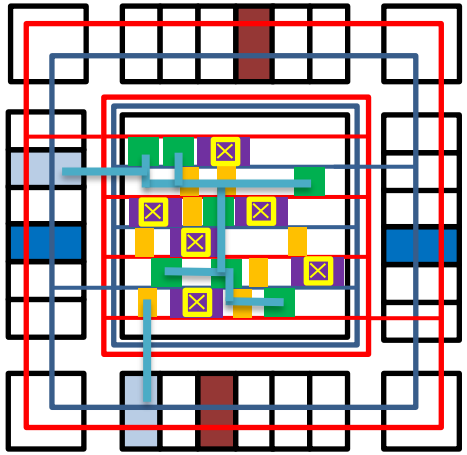
Планирование цепей питания
(Power planning)



Размещение
(Placement)



Синтез тактового дерева
(Clock tree synthesis)

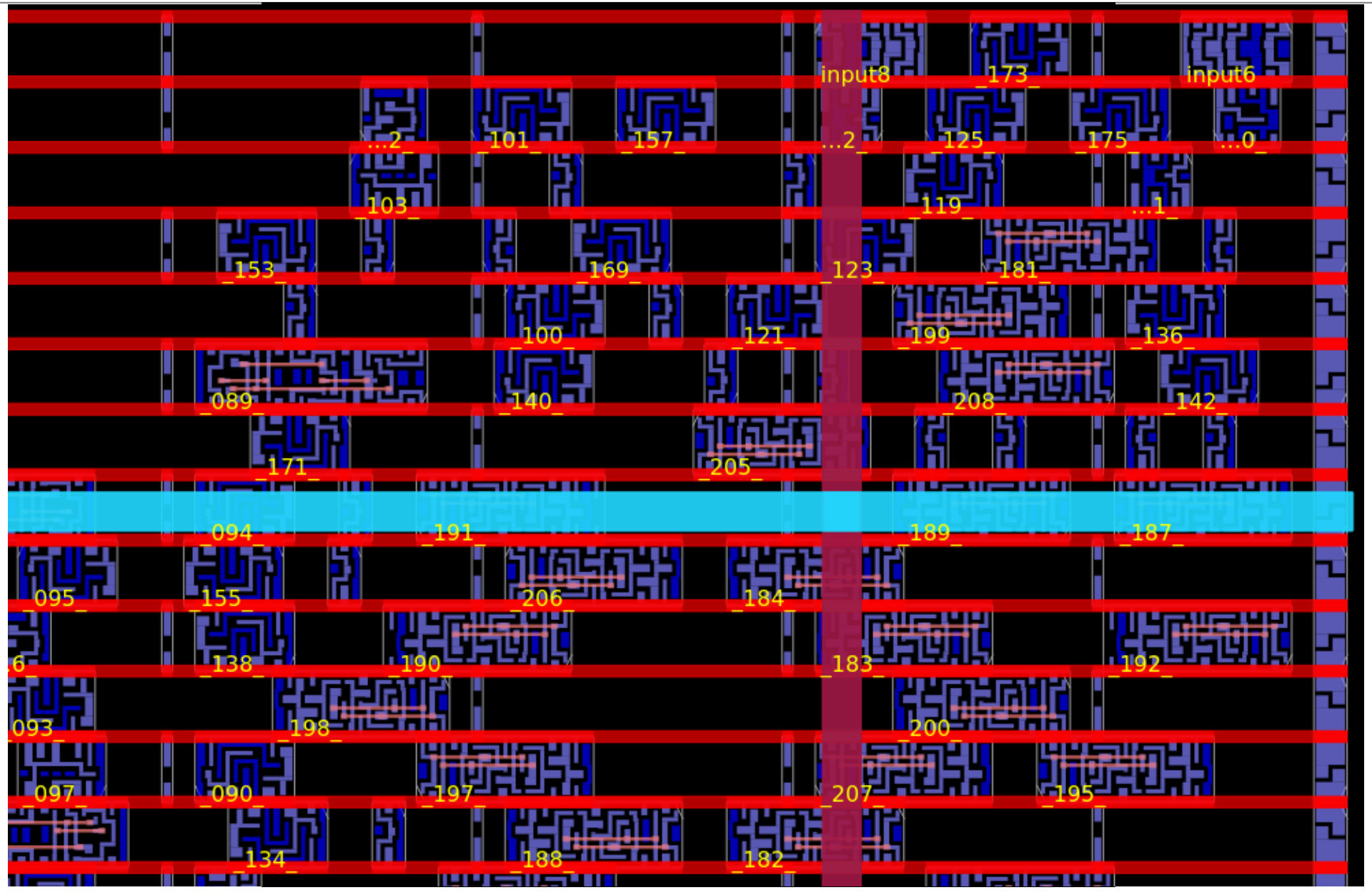


Трассировка
(Routing)

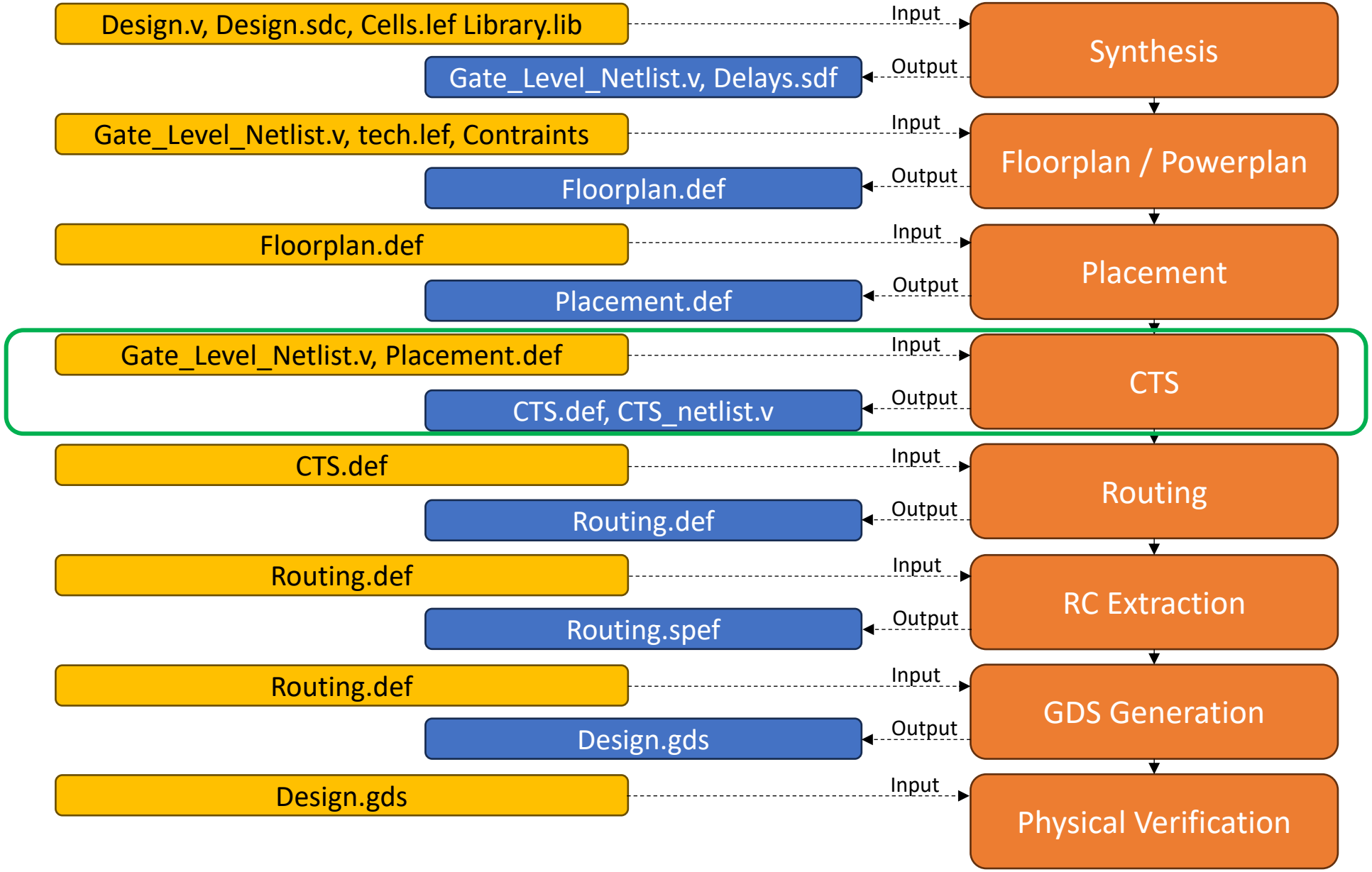
Результат размещения – файл формата DEF

```
COMPONENTS 3892 ;
    - FILLER_0_109 sky130_fd_sc_hd__decap_3 + SOURCE DIST + PLACED ( 55660 10880 ) N ;
    - FILLER_0_113 sky130_fd_sc_hd__decap_8 + SOURCE DIST + PLACED ( 57500 10880 ) N ;
    - FILLER_0_121 sky130_fd_sc_hd__fill_1 + SOURCE DIST + PLACED ( 61180 10880 ) N ;
    - FILLER_0_126 sky130_ef_sc_hd__decap_12 + SOURCE DIST + PLACED ( 63480 10880 ) N ;
...
    - _095_ sky130_fd_sc_hd__mux2_1 + PLACED ( 141220 176800 ) FS ;
    - _096_ sky130_fd_sc_hd__or2b_1 + PLACED ( 139840 174080 ) N ;
    - _097_ sky130_fd_sc_hd__o211a_1 + PLACED ( 141220 168640 ) FN ;
    - _098_ sky130_fd_sc_hd__mux4_1 + PLACED ( 148580 157760 ) FN ;
    - _099_ sky130_fd_sc_hd__and2b_1 + PLACED ( 148580 163200 ) FN ;
    - _100_ sky130_fd_sc_hd__mux2_1 + PLACED ( 161460 187680 ) FS ;
    - _101_ sky130_fd_sc_hd__mux2_1 + PLACED ( 160080 195840 ) N ;
    - _102_ sky130_fd_sc_hd__or2b_1 + PLACED ( 155480 195840 ) N ;
    - _103_ sky130_fd_sc_hd__o211a_1 + PLACED ( 155020 193120 ) FS ;
...
```

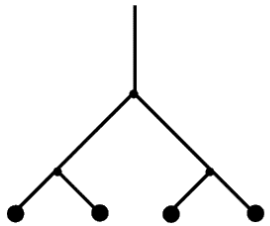
Результат размещения



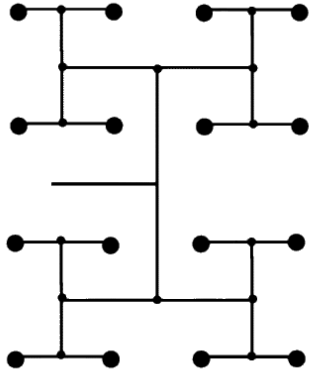
Этапы открытого маршрута OpenLane: генерация тактовых деревьев



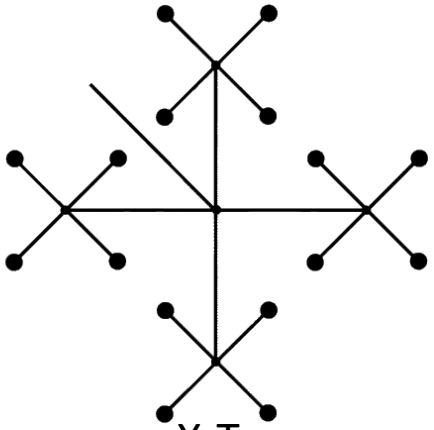
Виды деревьев синхронизации



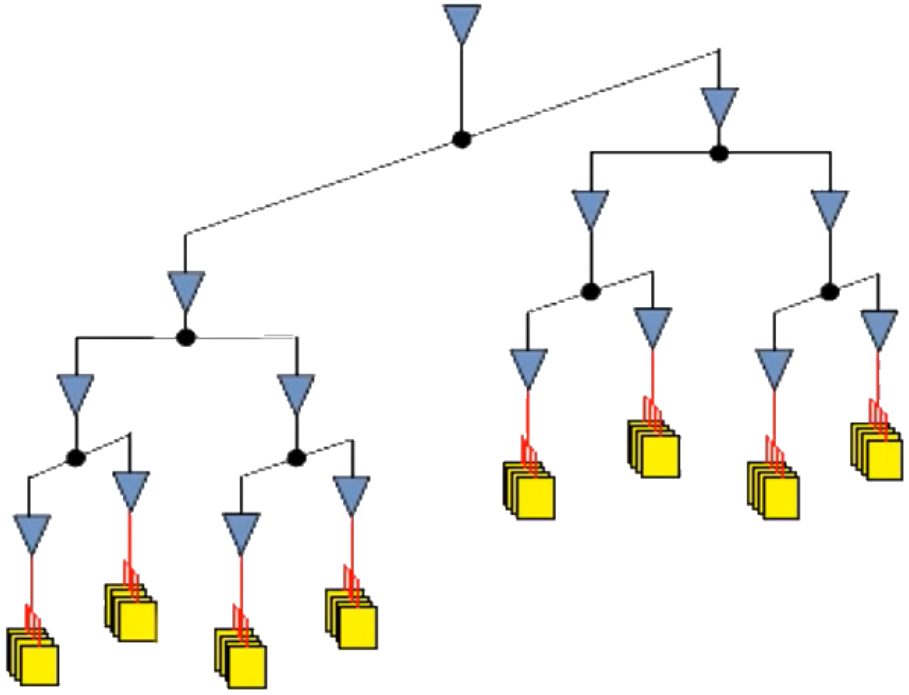
Y-Tree

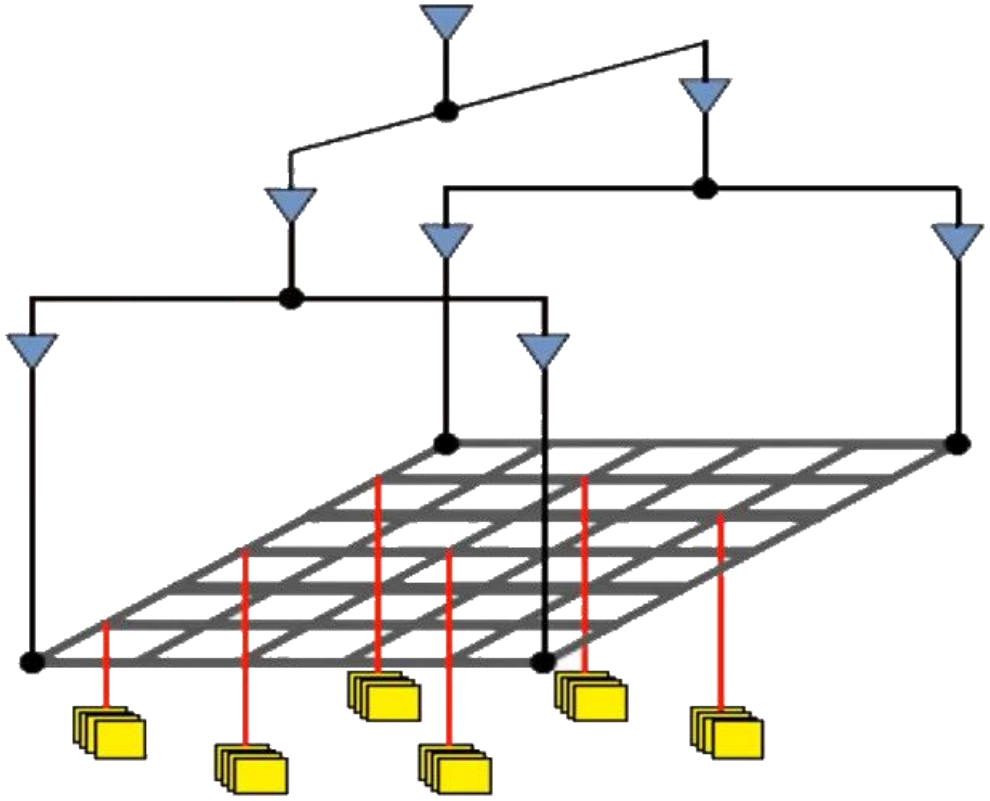


H-Tree



X-Tree

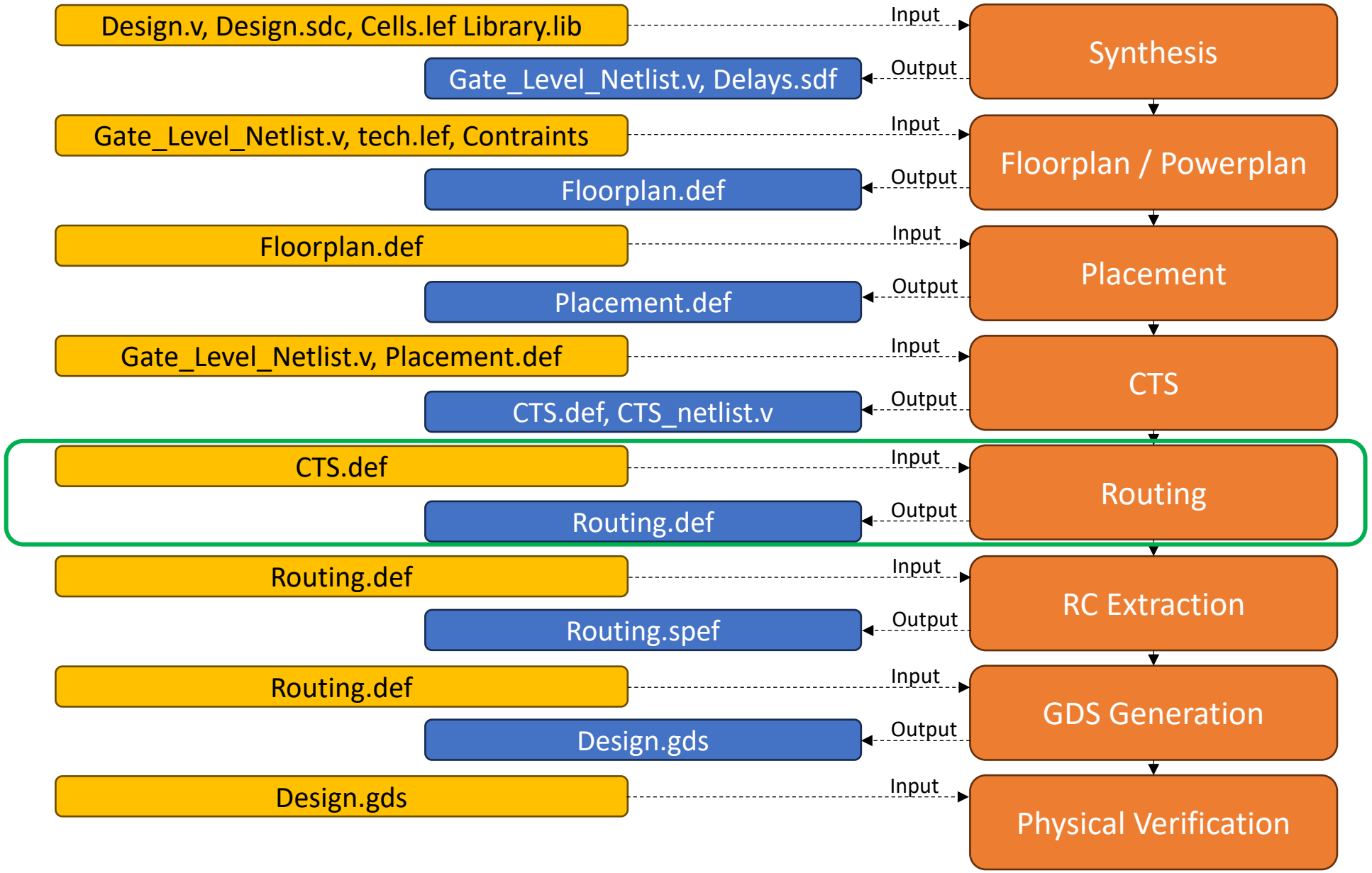




Запись о цепях синхронизации в DEF

```
- clk ( PIN clk ) ( clkbuf_0_clk A ) + USE CLOCK
    + ROUTED met3 ( 672750 680340 ) ( 691380 * 0 )
    NEW met1 ( 651130 371110 ) ( * 371790 )
    NEW met1 ( 651130 371790 ) ( 657570 * )
    NEW met1 ( 657570 371110 ) ( * 371790 )
    NEW met1 ( 657570 371110 ) ( 672750 * )
    NEW met2 ( 672750 371110 ) ( * 680340 )
    NEW met1 ( 508530 370770 ) ( * 371450 )
    NEW met1 ( 590410 371110 ) ( * 372130 )
    NEW met1 ( 590410 372130 ) ( 609270 * )
    NEW met2 ( 609270 371110 ) ( * 372130 )
    NEW met1 ( 609270 371110 ) ( 651130 * )
    NEW met2 ( 475410 370770 ) ( * 370940 )
    ...
```

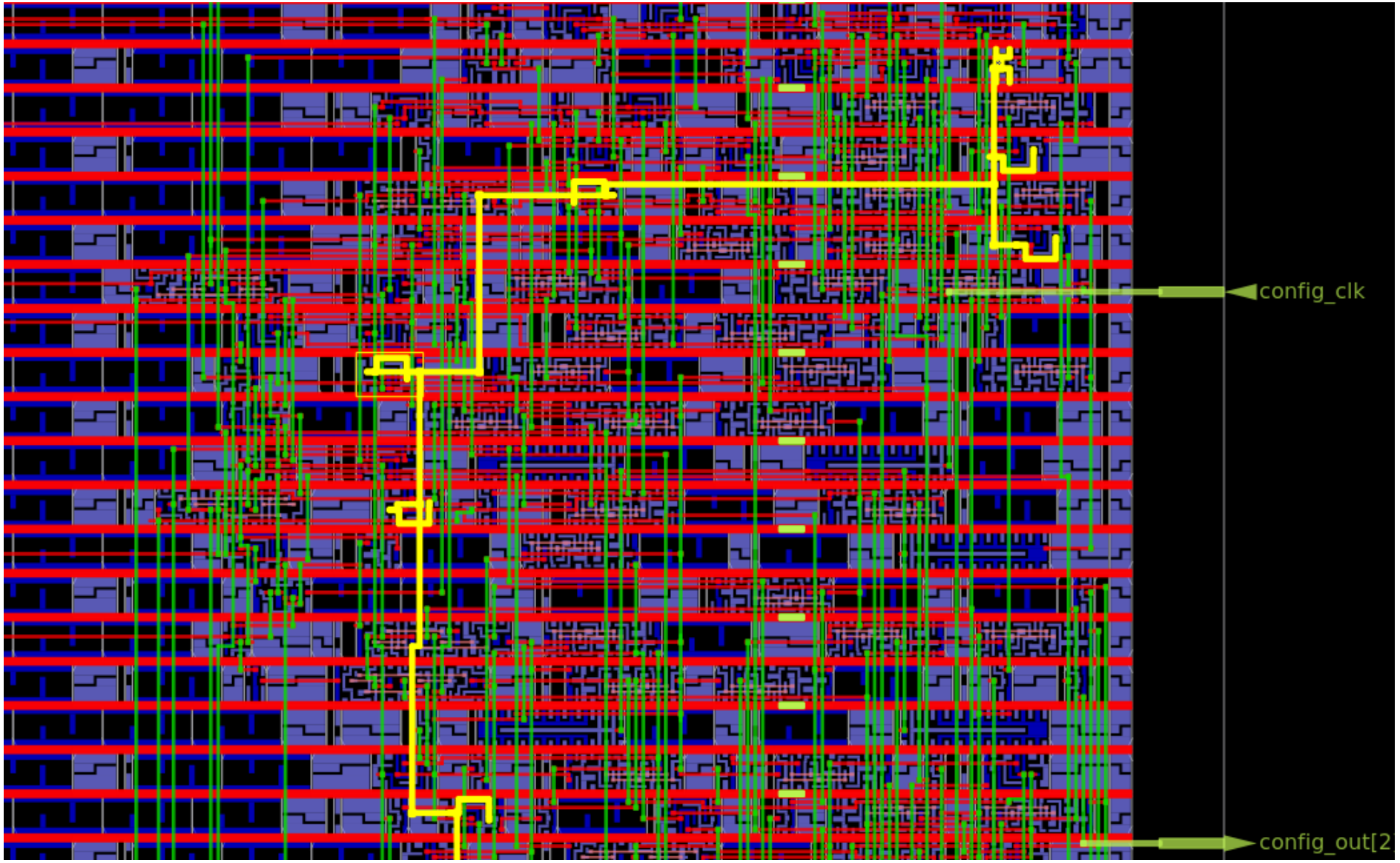
Этапы открытого маршрута OpenLane: трассировка



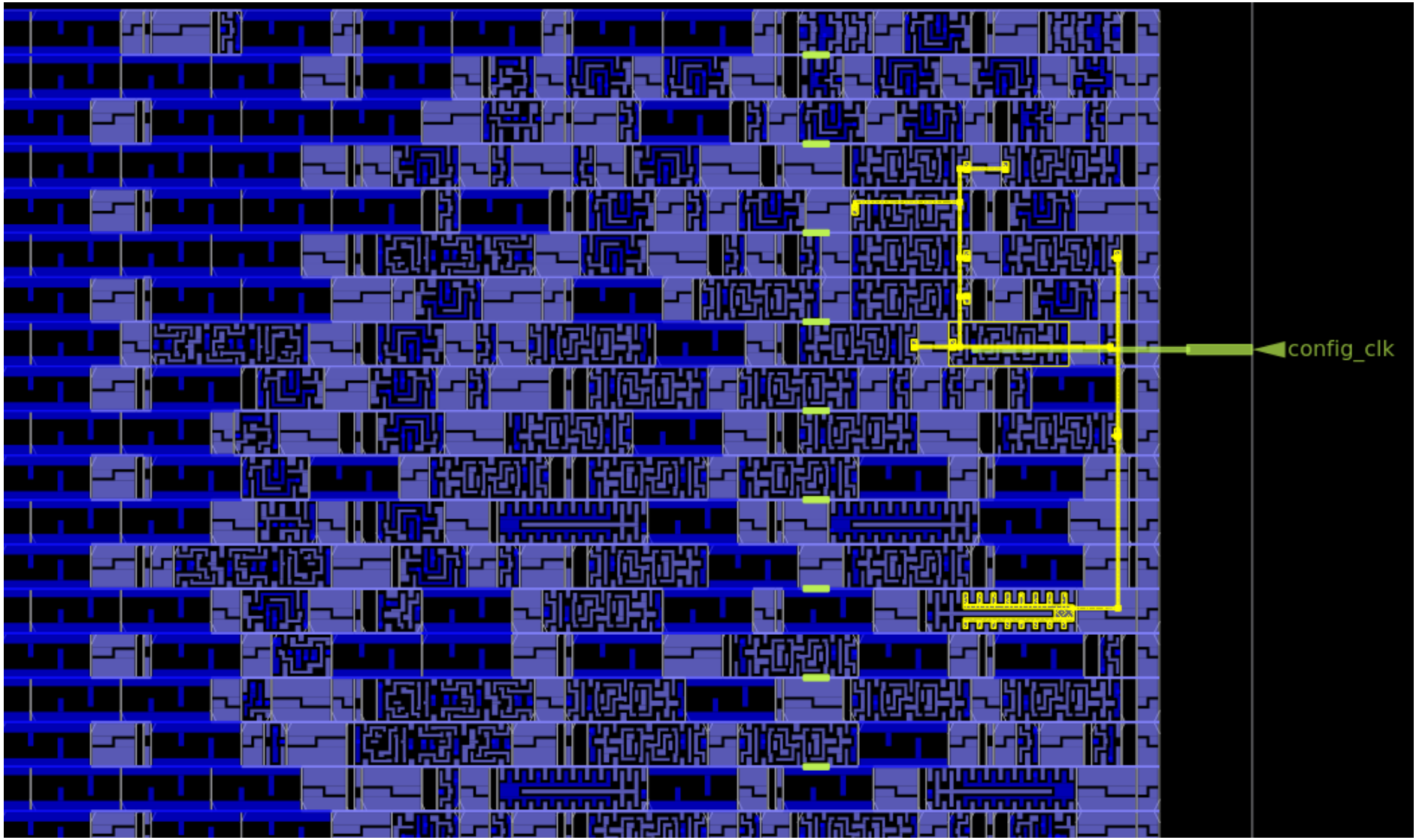
Результат трассировки – обновлённый файл DEF

```
NETS 168 ;
- net15 ( input15 X ) ( _157_ A1 ) + USE SIGNAL
      + ROUTED met2 ( 168590 197370 ) ( * 199410 )
      NEW met1 ( 78890 199410 ) ( 168590 * )
      NEW li1 ( 78890 199410 ) L1M1_PR_MR
      NEW li1 ( 168590 197370 ) L1M1_PR_MR
      NEW met1 ( 168590 197370 ) M1M2_PR
      NEW met1 ( 168590 199410 ) M1M2_PR
      NEW met1 ( 168590 197370 ) RECT ( -355 -70 0 70 )  ;
 - net16 ( input16 X ) ( _159_ A1 ) + USE SIGNAL
      + ROUTED met1 ( 182390 15130 ) ( 192510 * )
      NEW met2 ( 182390 15130 ) ( * 139910 )
      NEW met1 ( 182390 15130 ) M1M2_PR
      NEW li1 ( 192510 15130 ) L1M1_PR_MR
      NEW li1 ( 182390 139910 ) L1M1_PR_MR
      NEW met1 ( 182390 139910 ) M1M2_PR
      NEW met1 ( 182390 139910 ) RECT ( -355 -70 0 70 )  ;
```

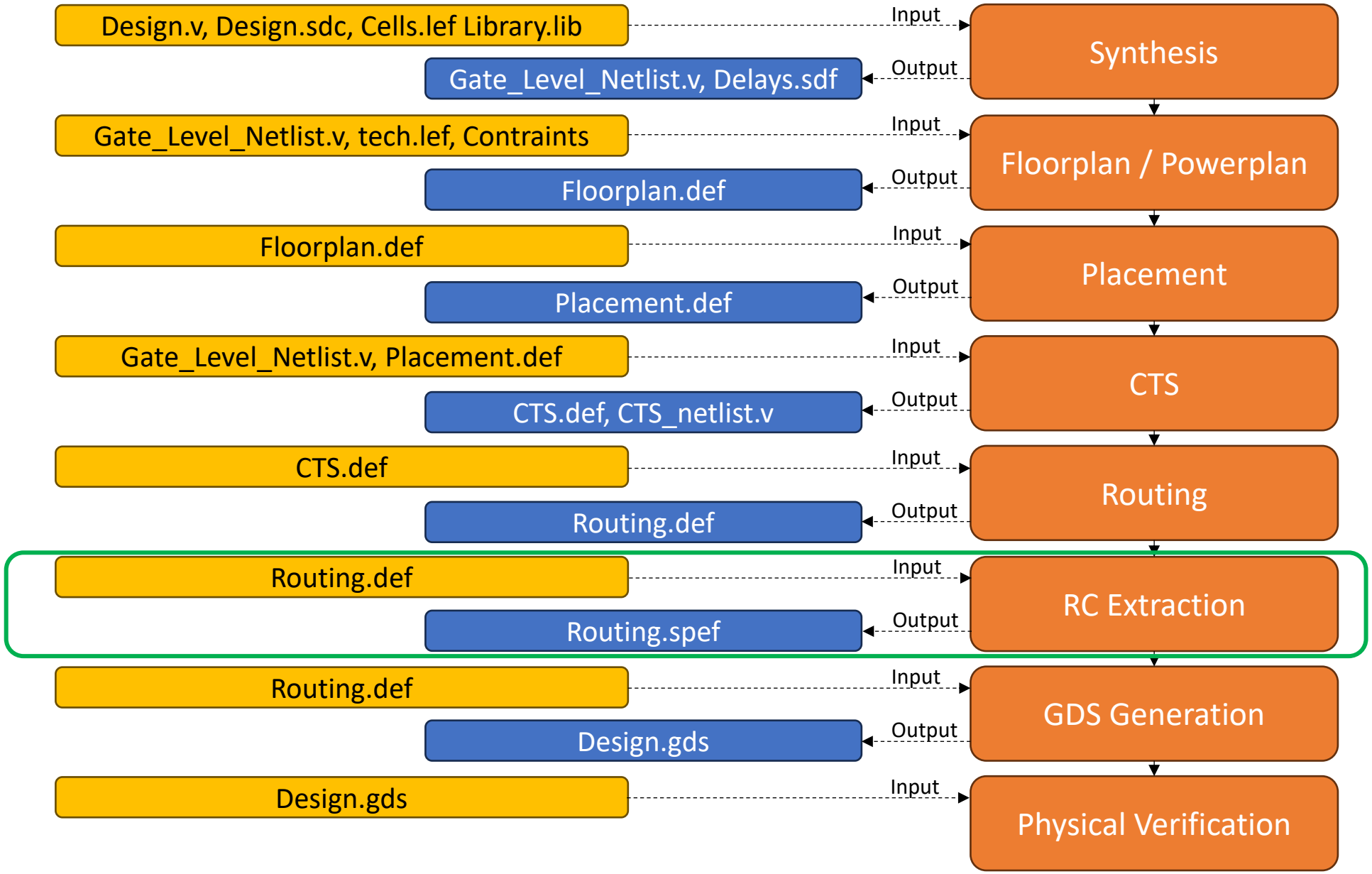
Результат P&R



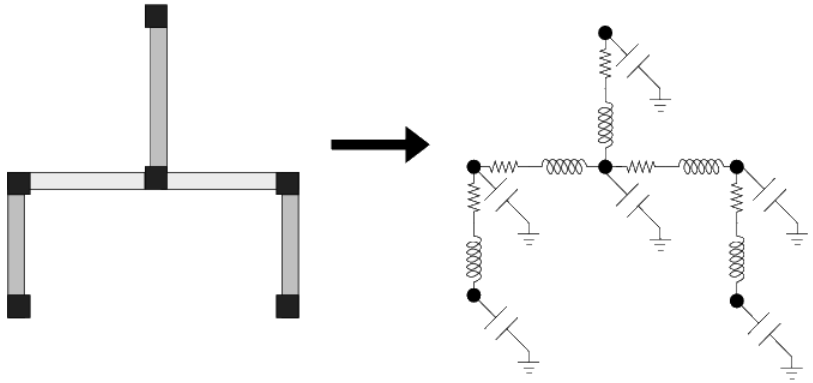
Тактовое дерево для схемы s44 из набора ISCAS'89

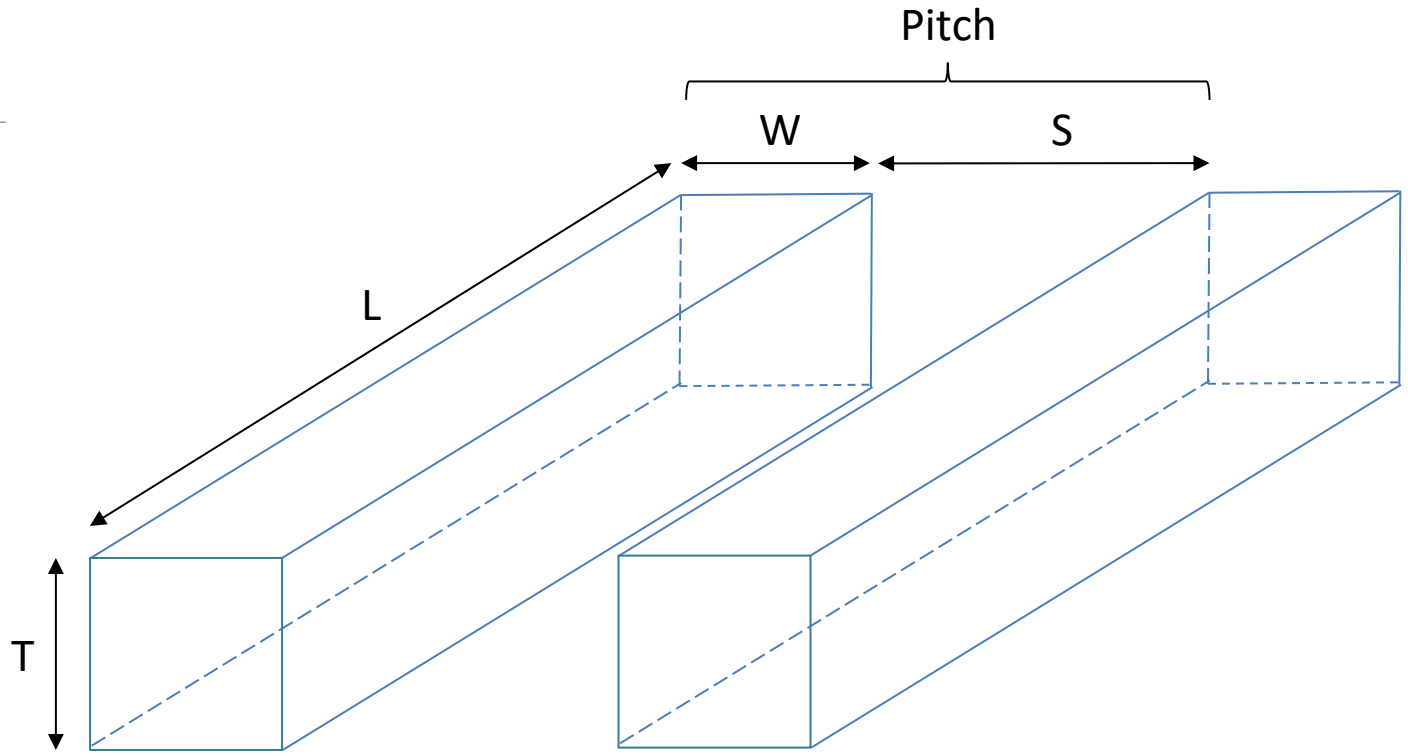


Этапы открытого маршрута OpenLane: экстракция паразитных элементов



Экстракция паразитных RC-элементов (1)





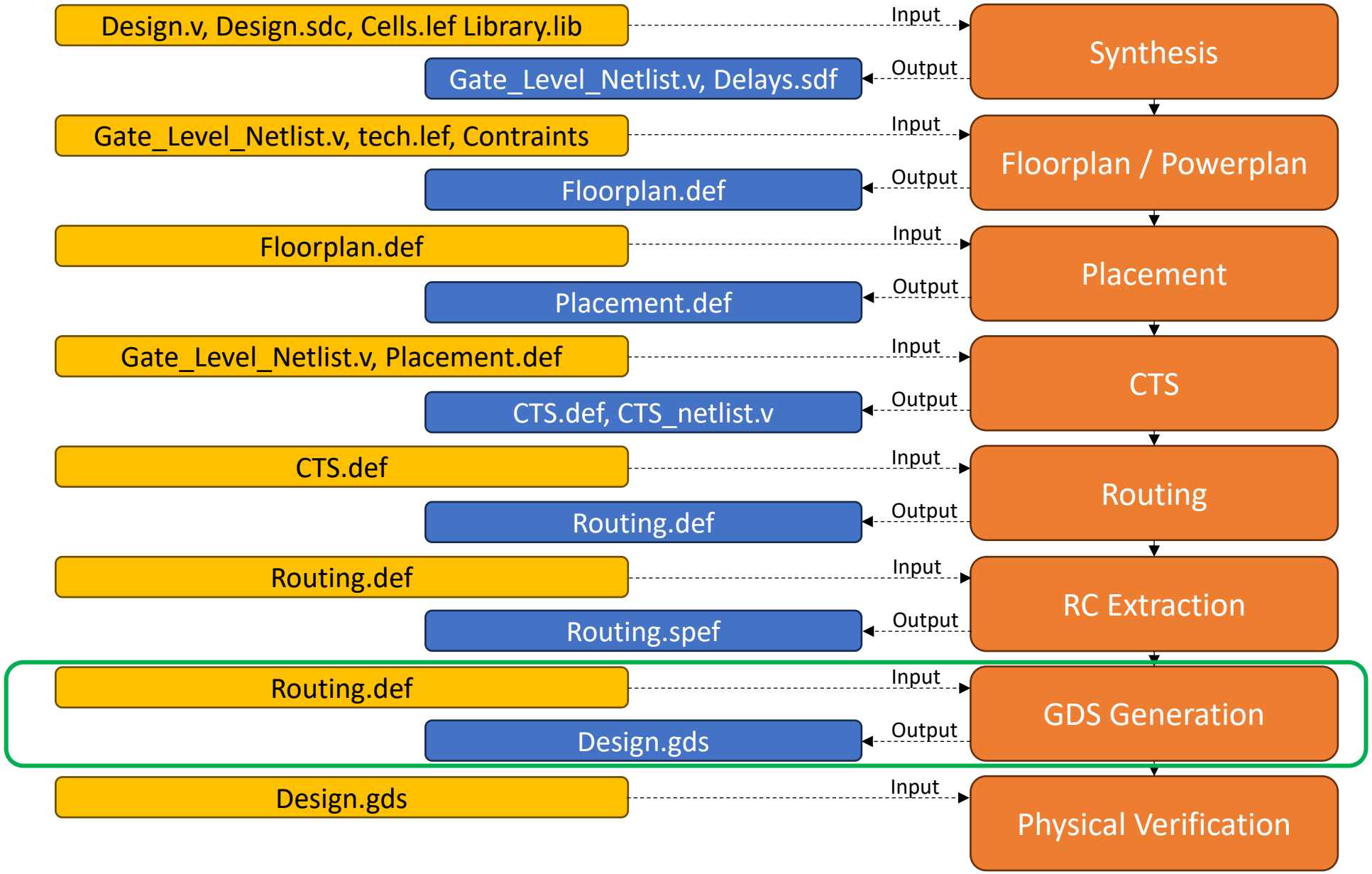
$$R = \frac{\rho}{T} \cdot \frac{L}{W}$$

$$C = \frac{\varepsilon}{T} \cdot \frac{L}{W}$$

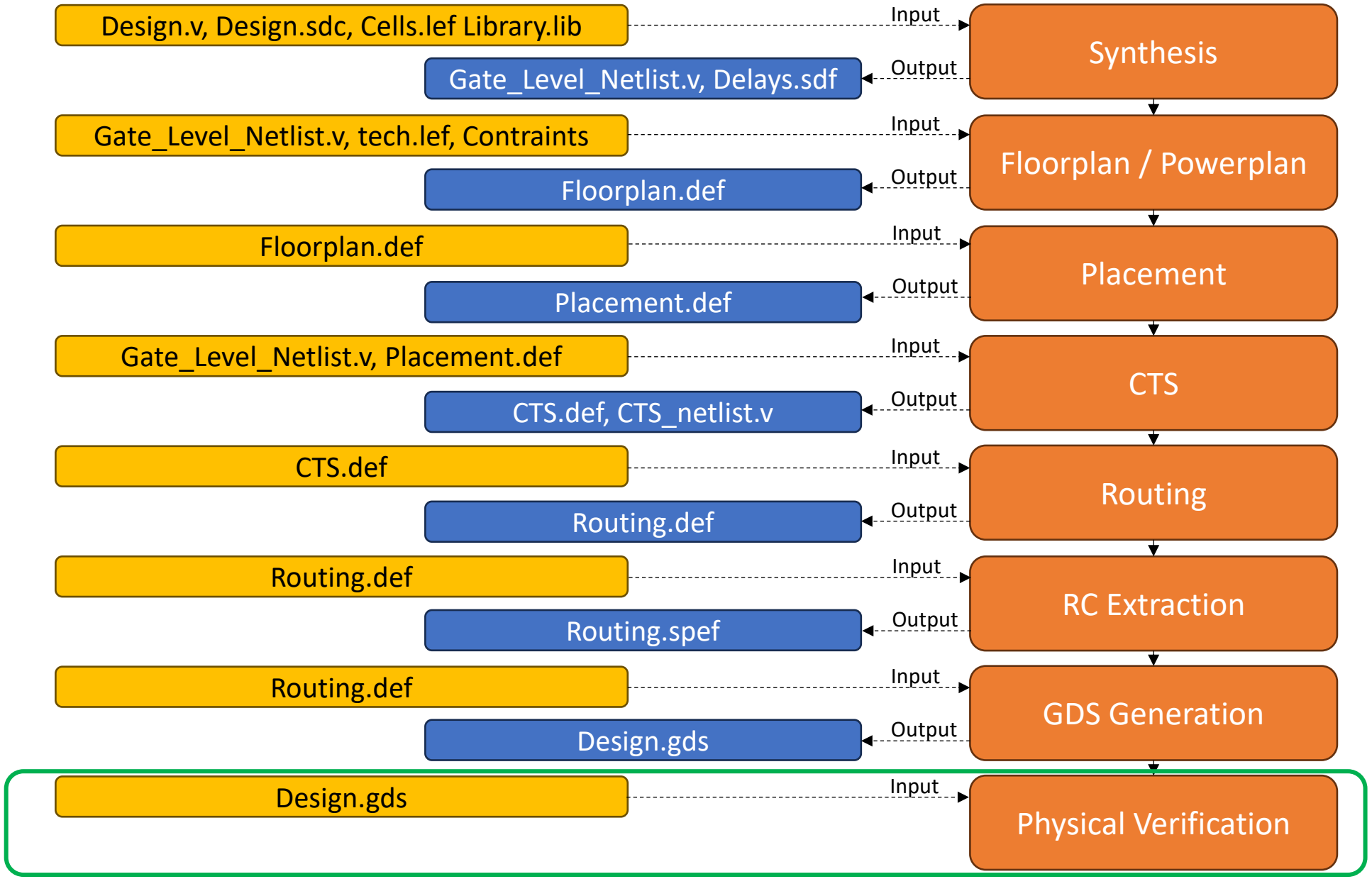
Время распространения сигнала:

$$\tau = R \cdot C$$

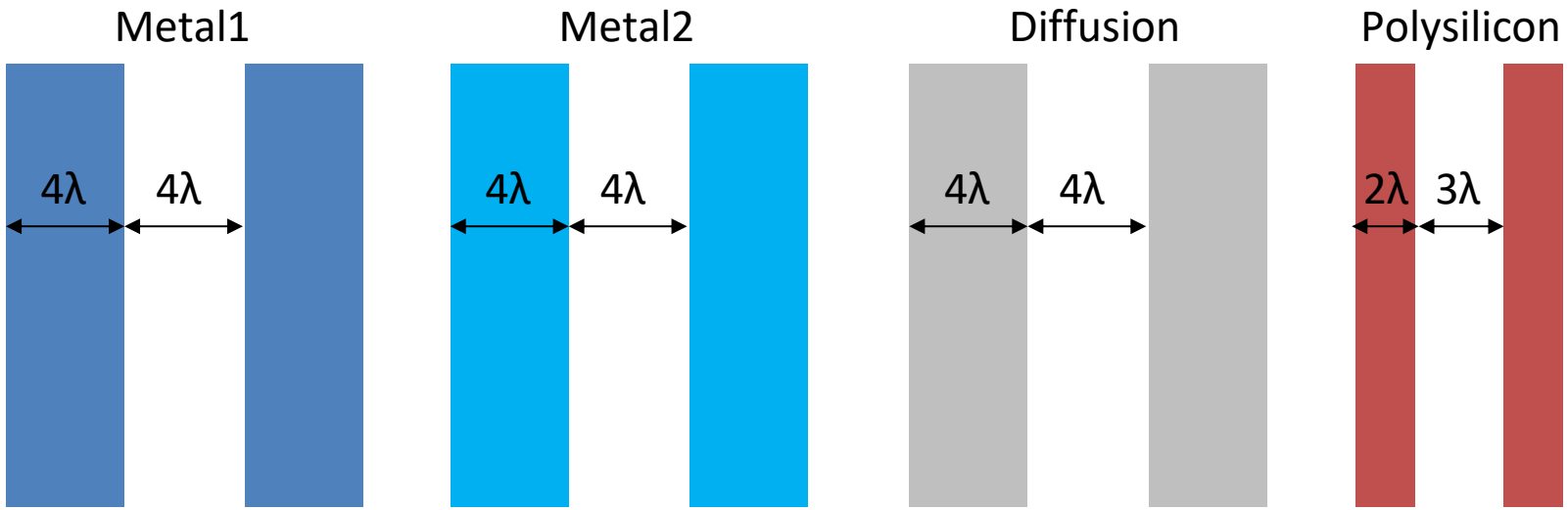
Этапы открытого маршрута OpenLane: генерация топологии в целом

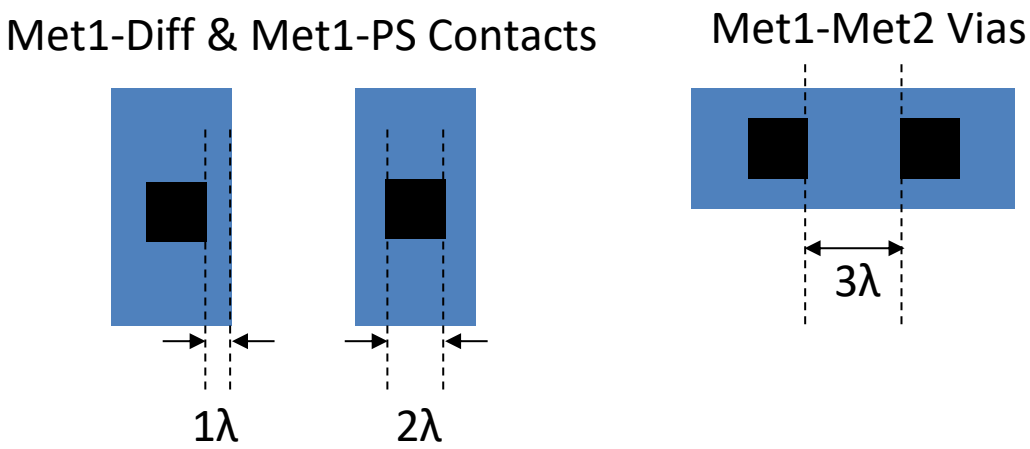


Этапы открытого маршрута OpenLane: физическая верификация



Проверка правил проектирования (Design Rule Check, DRC)

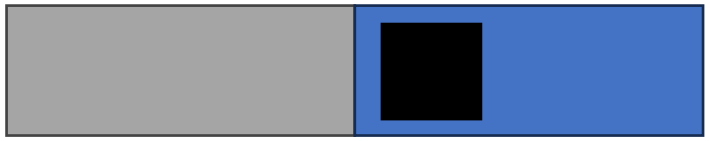




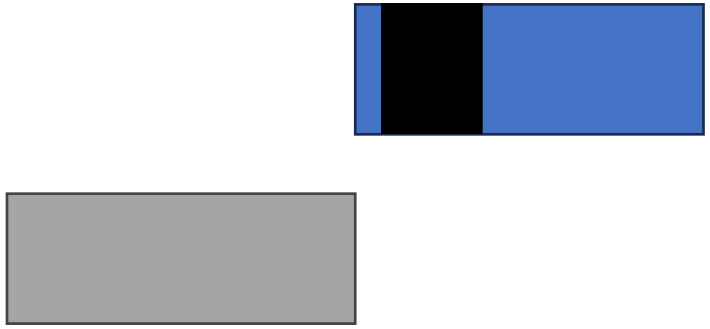
Electrical Rule Check (ERC) (1)

CrossTalk - пример лога с ошибками

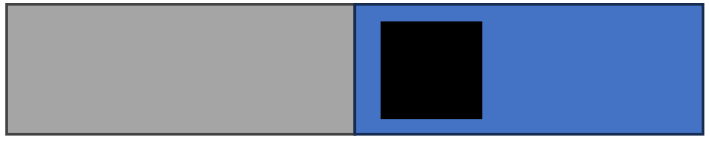
Топология, вид сверху:



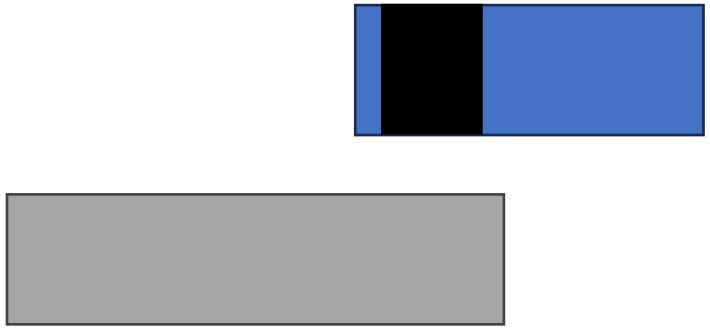
Металлы, вид сбоку:



Топология, вид сверху:

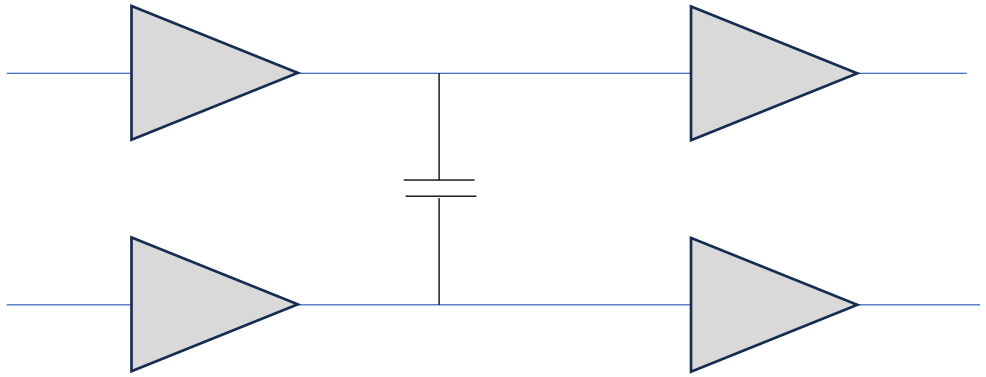


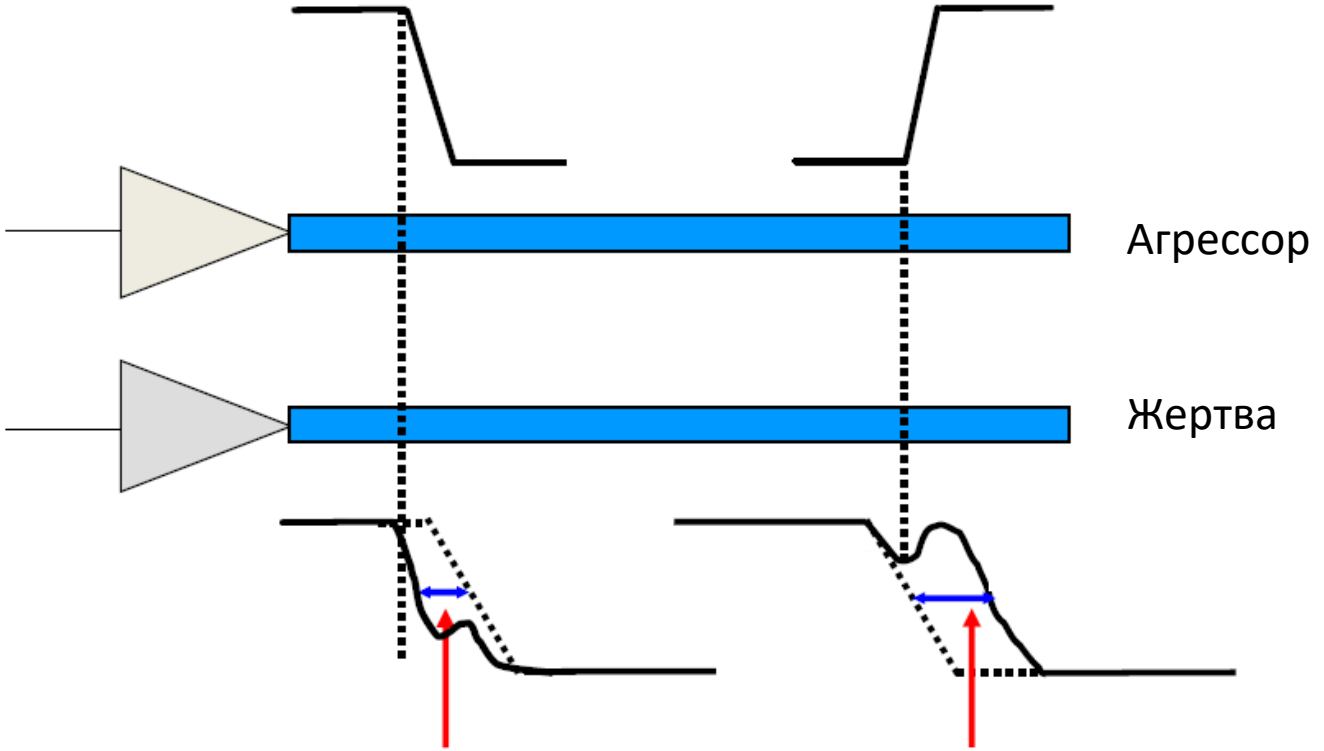
Металлы, вид сбоку:



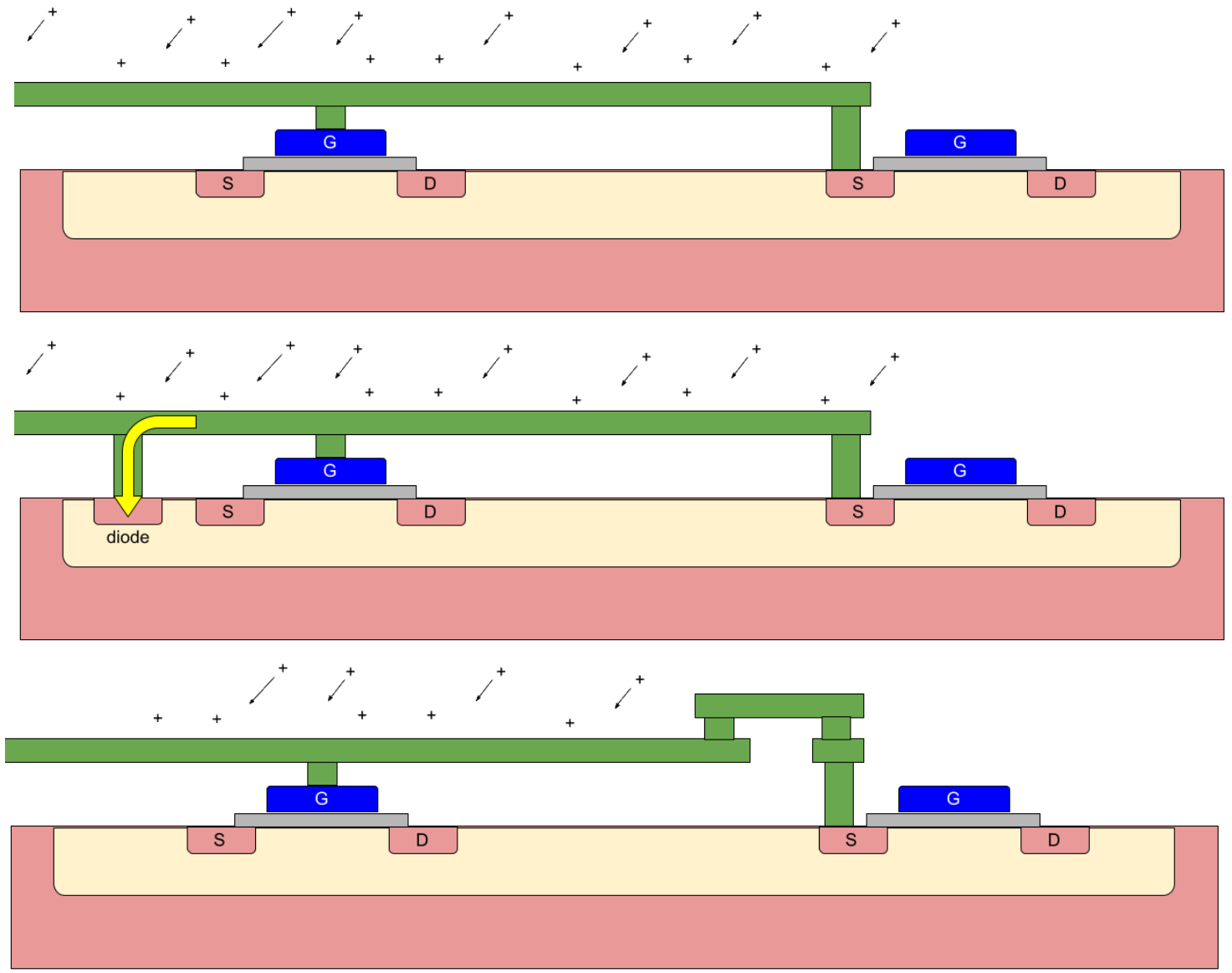
Electrical Rule Check (ERC) (2)

Signal Integrity

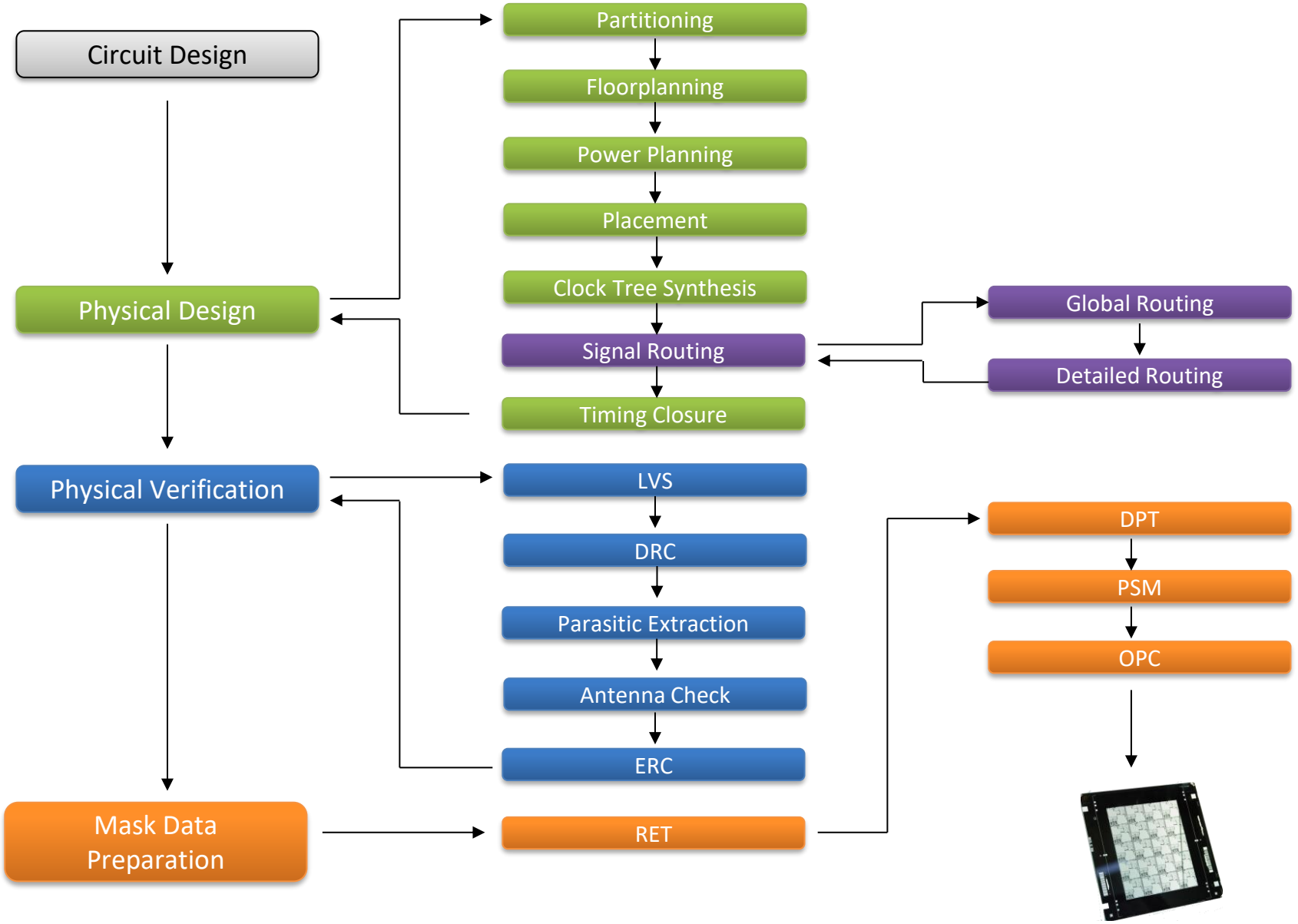




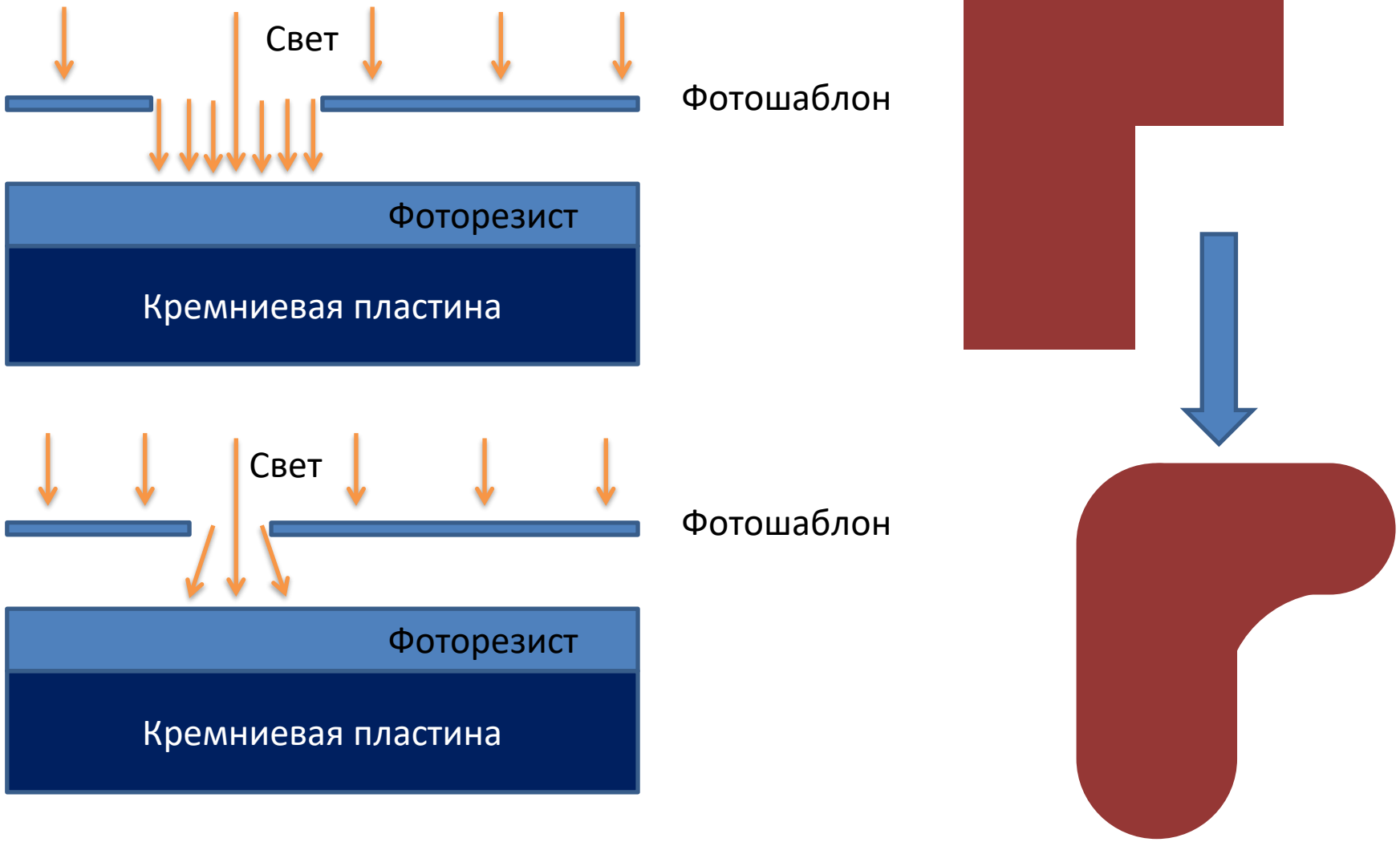
Проверка нарушений антенных правил



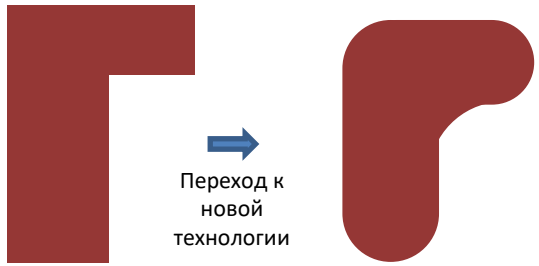
Результат работы маршрута OpenLane

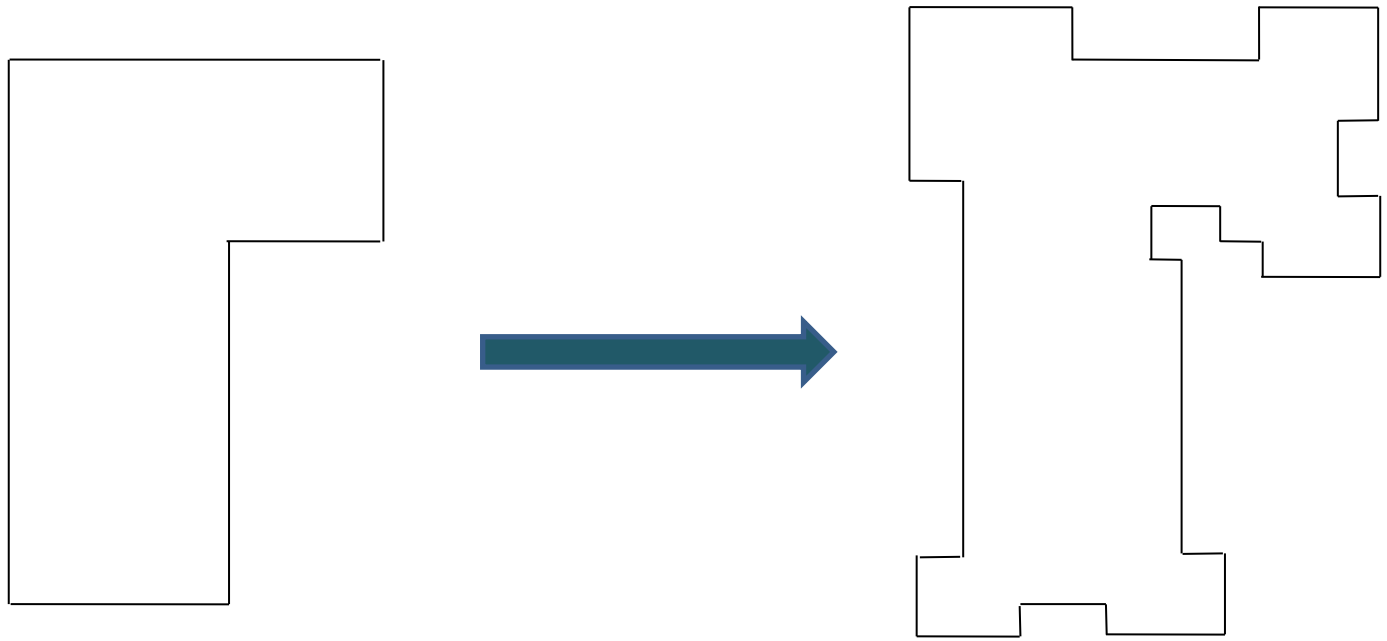


Коррекция оптической близости (Optical Proximity Correction, OPC) (1)

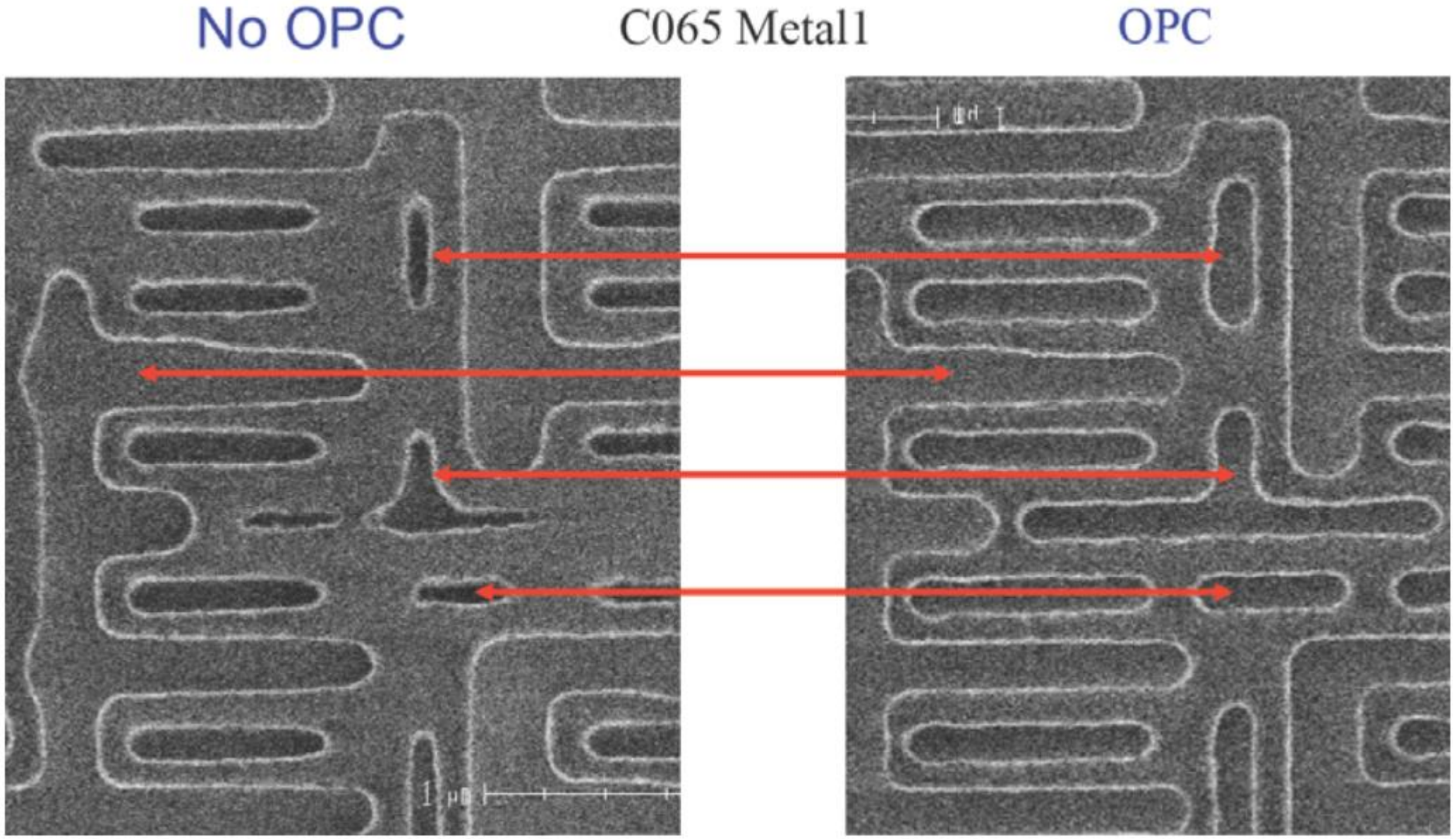


Коррекция оптической близости (Optical Proximity Correction, OPC) (2)

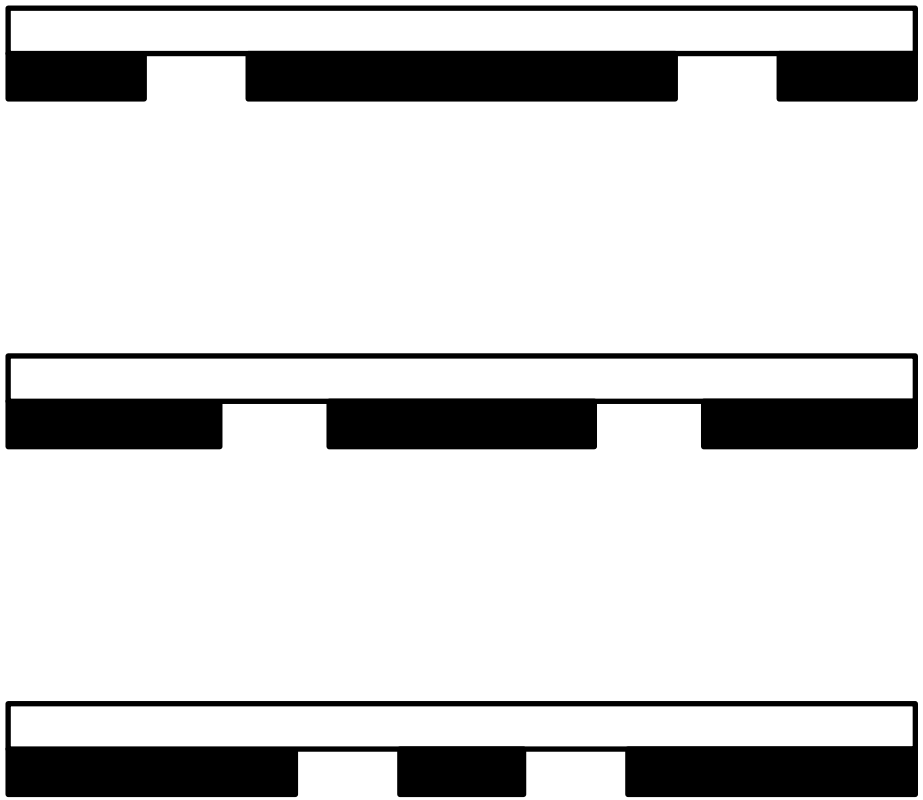


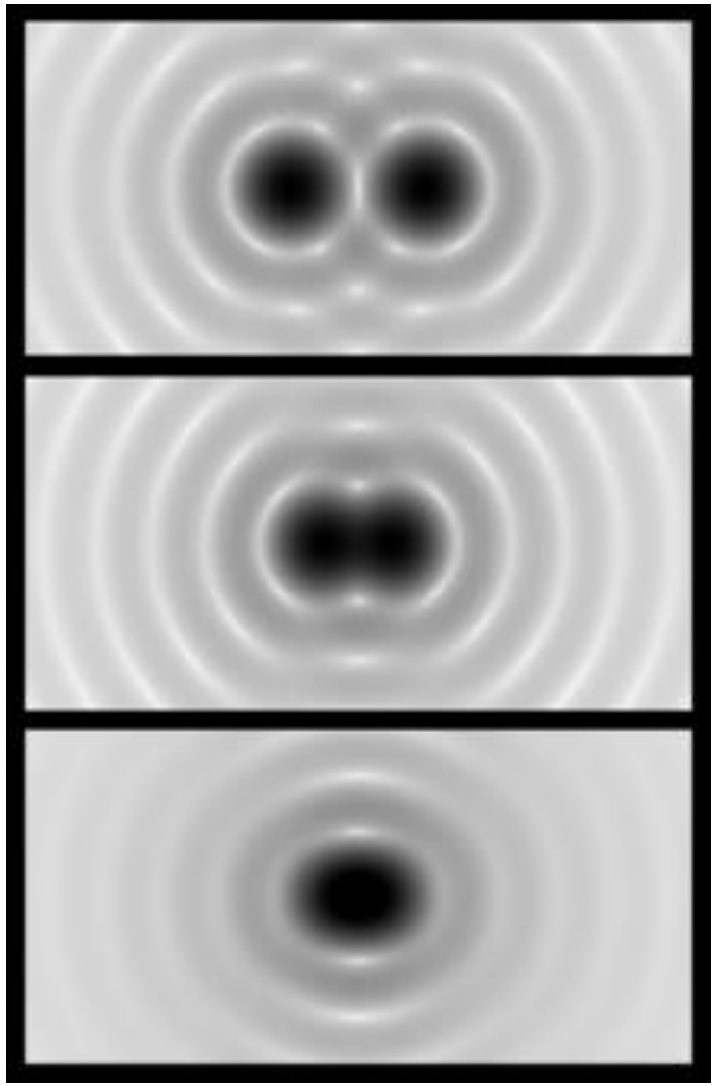


Коррекция оптической близости (Optical Proximity Correction, OPC) (3)



RET: фазосдвигающие маски (1)



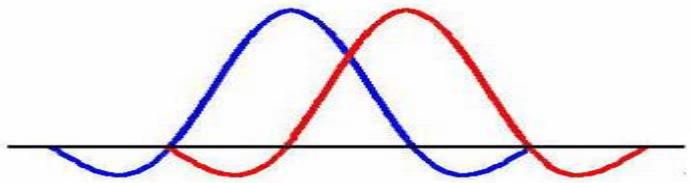


$$CD = k \cdot \frac{\lambda}{NA}$$

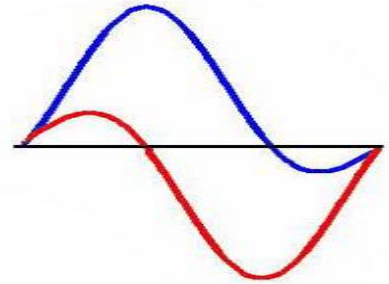
$$CD = 0{,}61 \cdot \frac{193nm}{NA}$$

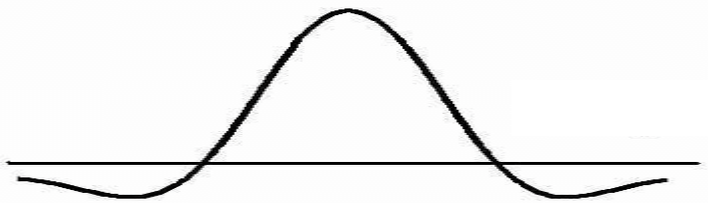
RET: фазосдвигающие маски (2)

Фотошаблон

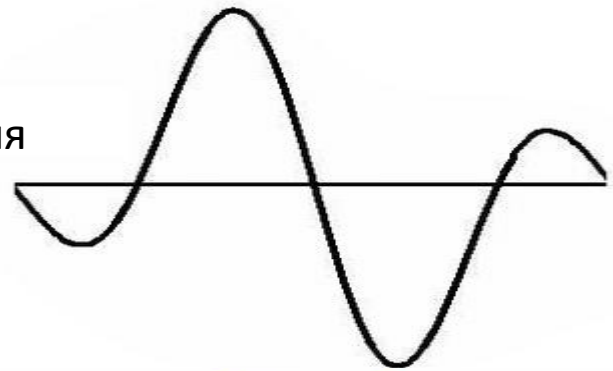


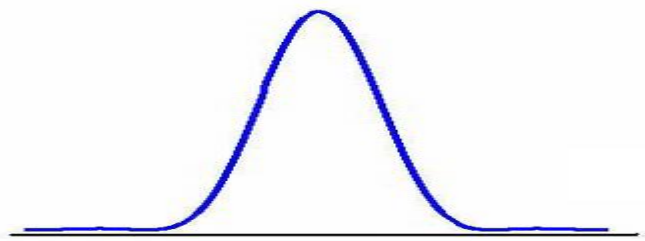
Амплитуда электромагнитного поля



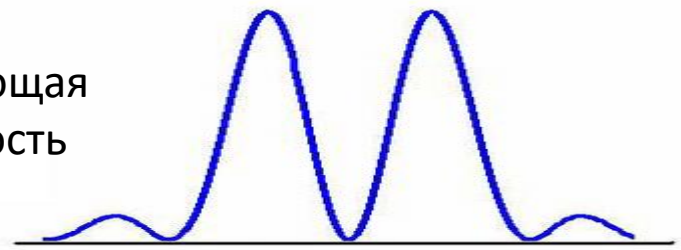


Суперпозиция волн

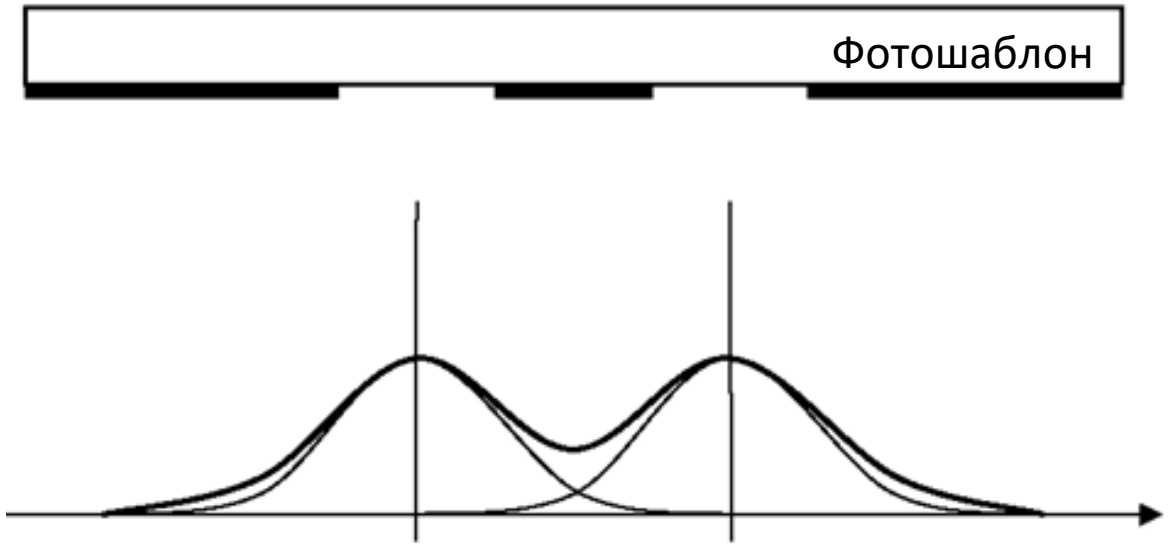


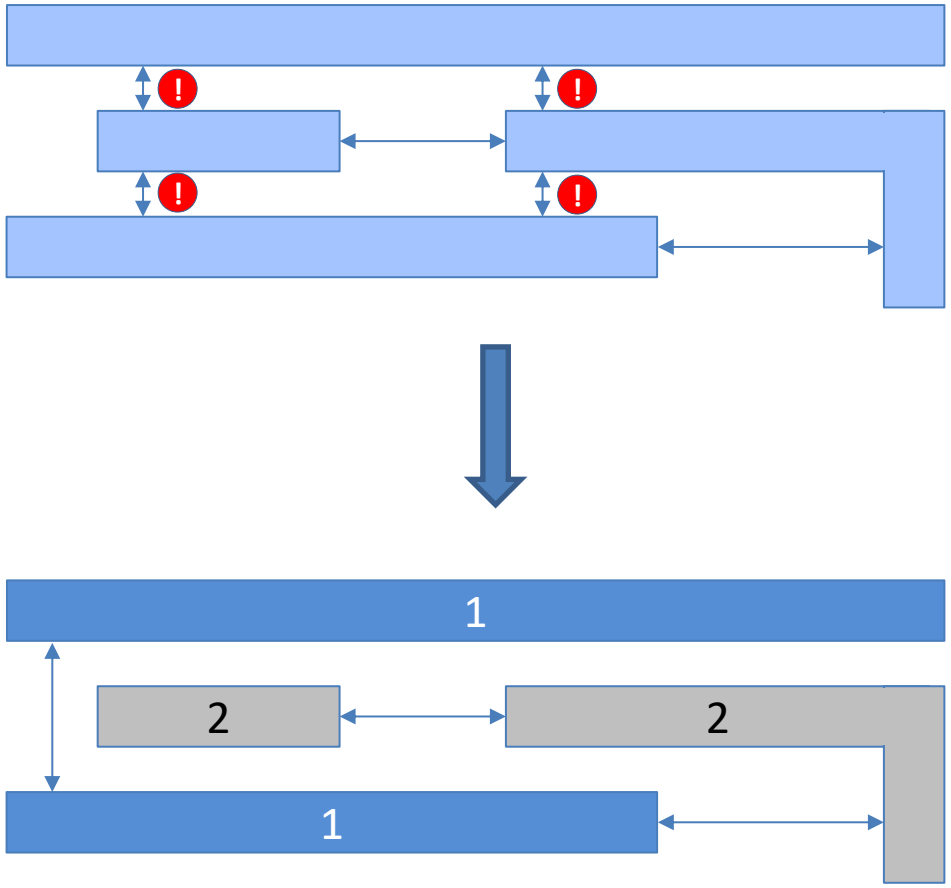


Результирующая интенсивность

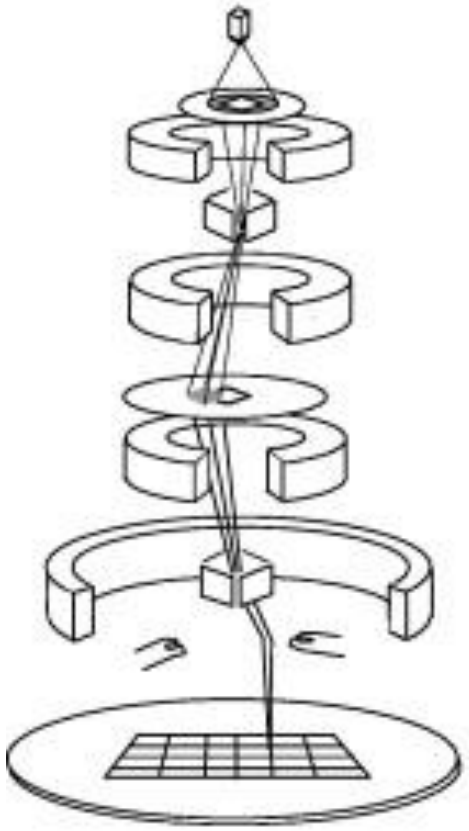


RET: технология двойного шаблона (Double Patterning Template, DPT)

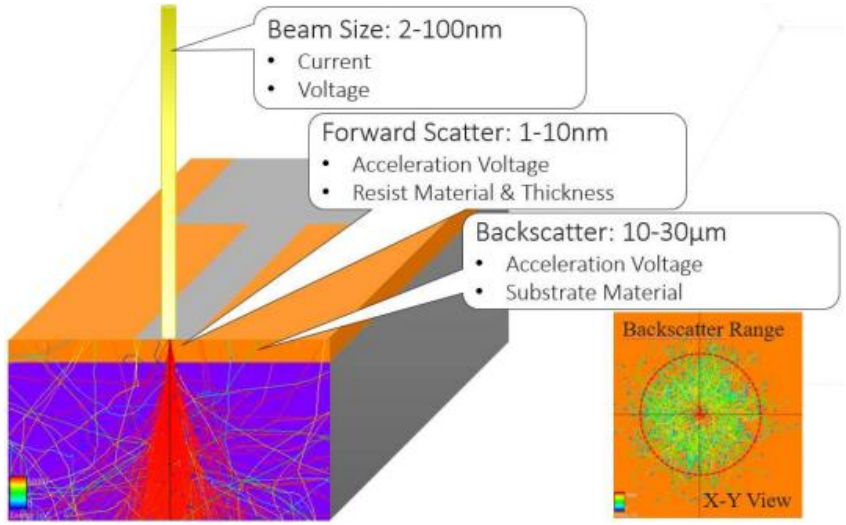




Решение проблем: Electron Beam Lithography (EBL)



Процессы в веществе



*Proximity Effect in E-Beam Lithography
https://www.genisys-gmbh.com/part-2-dose-pec-algorithm-and-parameter.html